

# Xilinx FPGA程序加载慢的原因和解决措施

[https://bbs.elecfans.com/jishu\\_1949548\\_1\\_1.html](https://bbs.elecfans.com/jishu_1949548_1_1.html)

如果是从spi flash启动的话，需要提高SPI的速度，具体做法就是在约束里面增加语句：

```
set_property BITSTREAM.CENERAL.COMPRESS TRUE [current_design]
set_property CFGBVS VCC0 [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]

set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4 [current_design]
set_property CONFIG_MODE SPIx4 [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 50 [current_design]
```

*#vivado管脚约束XDC文件*

*#FPGA\_CLK*

```
set_property PACKAGE_PIN H16 [get_ports CLK_i]
set_property IOSTANDARD LVCMOS33 [get_ports CLK_i]
```

*#rst\_n*

```
set_property PACKAGE_PIN T19 [get_ports RSTn_i]
set_property IOSTANDARD LVCMOS33 [get_ports RSTn_i]
```

*#LED\_o*

```
set_property PACKAGE_PIN J16 [get_ports {LED_o[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {LED_o[3]}]
set_property PACKAGE_PIN K16 [get_ports {LED_o[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {LED_o[2]}]
set_property PACKAGE_PIN G15 [get_ports {LED_o[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {LED_o[1]}]
set_property PACKAGE_PIN H15 [get_ports {LED_o[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {LED_o[0]}]
```