1. gtx速度

	Type	Max Performance[1]	Max Transceivers	Peak Bandwidth[2]
Versal ACAP	GTY/GTM	32.75/58.0	44/52	6,032Gb/s
Versal Premium Series	GTY/GTM	32.75/112.0	28/70	9,040Gb/s
Virtex® UltraScale+	GTY/GTM	32.75/58.0	128/48[3]	8,384Gb/s
Kintex® UltraScale+	GTH/GTY	16.3/32.75	44/32	3,268Gb/s
Virtex UltraScale	GTH/GTY	16.3/30.5	60/60	5,616Gb/s
Kintex UltraScale	GTH	16.3	64	2,086Gb/s
Virtex-7	GTX/GTH/GTZ	12.5/13.1/28.05	56/96/16[3]	2,784Gb/s
Kintex-7	GTX	12.5	32	800Gb/s
Artix®-7	GTP	6.6	16	211Gb/s
Zynq® UltraScale+	GTR/GTH/GTY	6.0/16.3/32.75	4/44/28	3,268Gb/s
Zynq-7000	GTX	12.5	16	400Gb/s
Spartan-6	GTP	3.2	8	51Gb/s

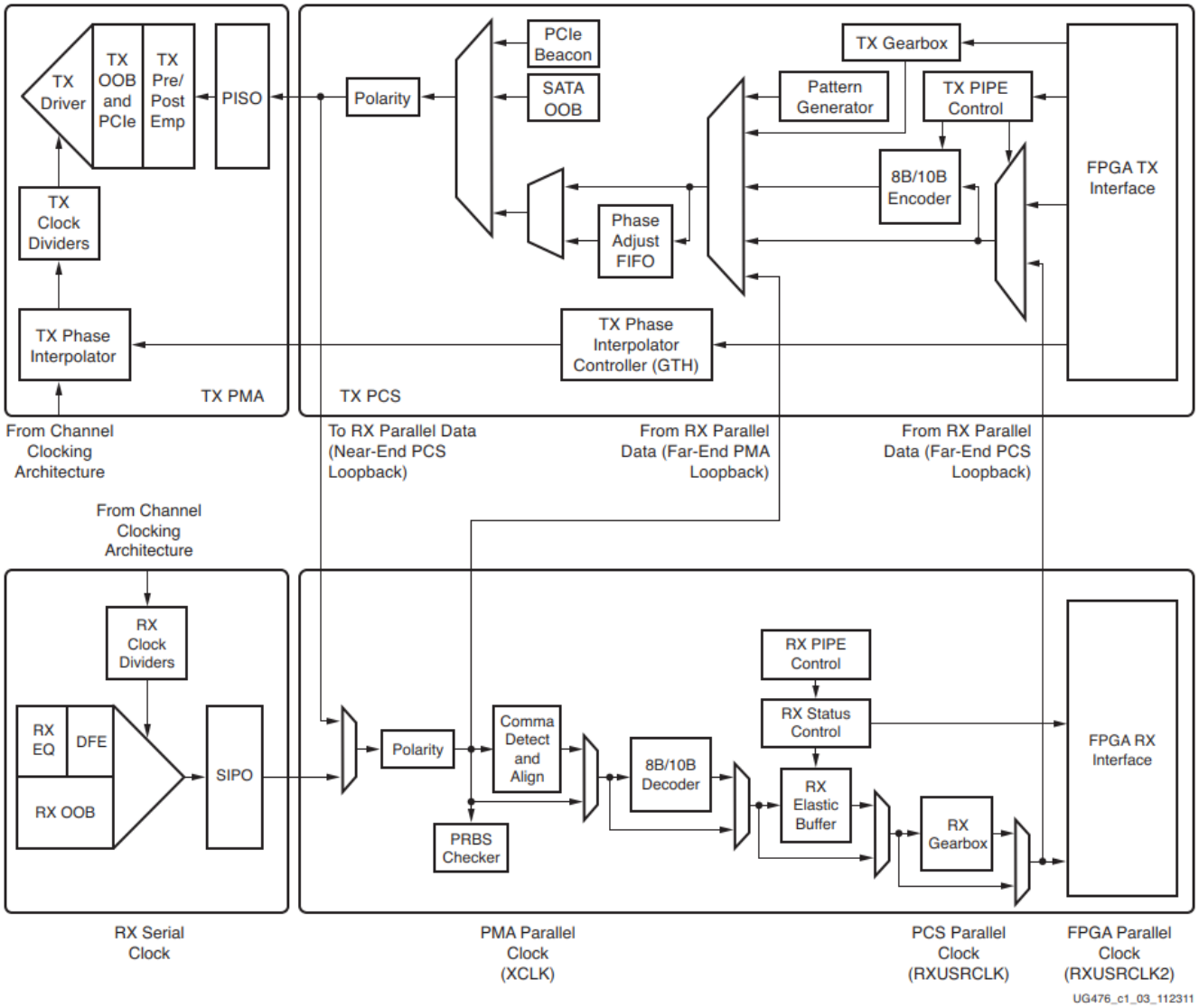

Figure 1-3: **GTXE2_CHANNEL Primitive Topology**

2. FMC卡接口标准

https://fmchub.github.io/appendix/VITA57_FMC_HPC_LPC_SIGNALS_AND_PINOUT.html

- ANSI/VITA 57.1 - Revised2019 FMC: FPGA Mezzanine Cards Base Standard
- ANSI/VITA 57.4 - Revised2018 FMC+: FPGA Mezzanine Cards Base Standard - Next Generation

Function	FMC	FMC+	FMC+ with HSPCe
Maximum # parallel I/Os	80 diff/160 single ended	80 diff/160 SE	80 diff/160 SE
Clocks	4	4	4
Maximum # GTs	10	24	32
GT clocks	2	6	8
Miscellaneous	JTAG, SYNC, power good, geographic address	JTAG, SYNC, power good, geographic address	JTAG, SYNC, power good, geographic address
Power supplies	V_{ADJ}* (4 pins), 3V3 (4 pins), 12V (2 pins), 3V3 Aux (1 pin)	V_{ADJ}* (4 pins), 3V3 (8 pins), 12V (4 pins), 3V3 Aux (1 pin)	V_{ADJ} (4 pins), 3V3 (8 pins), 12V (4 pins), 3V3 Aux (1 pin)

* V_{ADJ}: mezzanine defined for voltage level, but provided by host

Table 1 – Summary of FMC and FMC+ connectivity