

vcs使用

1. ucli

simv [simv_options] -ucli

```
% simv -ucli
ucli%
# 输入help可以查看命令
```

交互脚本方式: simv -ucli -i ucli_script.inc

交互脚本是tcl格式的，可以使用for循环。

```
for {set i 0} {$i < 8} {incr i} {
    force a 1
    run 10ns
    force a 0
    run 10ns
}
```

force 命令注意，只能force信号为具体的值，不能force一个信号到另外一个信号
force到的具体值需要给完整的宽度，比如8'd28, 不能直接给28, 可能会有宽度不匹配的问题，导致force失败。

2. 给register赋初始值

这是为了在netlist仿真的时候，有一些不带reset/set的register给其赋个初始值，避免X态传播。

```
+vcs+initreg+random option must be specified at compile time

# 以下可以在run simv时指定
+vcs+initreg+0
+vcs+initreg+1
+vcs+initreg+random // 采用赋随机值
+vcs+initreg+seed_value
```

3. 后仿时timing violation避免产生X态

在编译时加上+no_notifier 选项。

4. plusargs

```
initial begin
  if($test$plusargs("test")) begin
    $display("haha");
  end
end
```

```
./simv+test
```

5. 反标率

```
% vcs -diag=sdf:verbose example.v
% simv
% cat sdfAnnotateInfo
The following is the output:
Static entries in elaborated design under "test":
    Annotated by SDF "example.sdf":
    No. of Pathdelays   = 4   Annotated = 50.00%
    No. of Tchecks     = 4   Annotated = 50.00%
                                     Total           Annotated
Percentage
    IOPATH              4           2
50.00%
    Path Delays Summary of above
    SETUPHOLD          4           2
50.00%
    Timing checks Summary of above

OverAll Static entries in elaborated design:
    No. of Pathdelays   = 4   Annotated = 50.00%
    No. of Tchecks     = 4   Annotated = 50.00%
                                     Total           Annotated
Percentage
    IOPATH              4           2
50.00%
    Path Delays Summary of above
```

6. kdb

```
# VCS Two-step Flow Compilation:
% vcs -debug_access+r -sverilog -kdb top.v

# VCS Three-step Flow Compilation:
% vlogan top.v -kdb
```

```
% vcs top -debug_access+r -kdb
```

7. rand seed

```
reg    [31:0]  seed;
reg    [31:0]  ret;
initial begin
    if ($value$plusargs("seed=%d",seed)) begin
        $display("seed = %0d", seed);
        ret = $urandom(seed);

        repeat(4) begin
            ret = $urandom();
            $display("ret = %0x", ret);
        end
        $finish;
    end
end
```

```
./simv +seed=21
seed = 21
ret = c7466bae
ret = cf3f2455
ret = ff0b7390
ret = 5cbc21bd
```

```
./simv +seed=22
seed = 22
ret = 4c85682
ret = 2c3fd11a
ret = 6f1599cc
ret = 7098322c
```