

## 1. user check

### 1.1 vc\_check.tcl

```
set search_path "."
set link_library " "

analyze -format sverilog -vcs "chip.v"
elaborate chip

foreach_in_collection cell [get_cells] {
    set cell_name [get_object_name $cell]
    set ref_name [get_attribute -objects $cell -name ref_name];
    set orig_ref_name [regsub {_\d\d\d\d} $ref_name {}]
    puts "cell_name: $cell_name, ref_name: $ref_name, orig_ref_name:
$orig_ref_name"
}
```

### 1.2 output

```
cell_name: core_0, ref_name: core, orig_ref_name: core
cell_name: core_1, ref_name: core, orig_ref_name: core
cell_name: core_2, ref_name: core_0000, orig_ref_name: core
cell_name: core_3, ref_name: core_0001, orig_ref_name: core
cell_name: out, ref_name: SEQ_FF, orig_ref_name: SEQ_FF
cell_name: I_OR_N_1, ref_name: BITWISE_OR, orig_ref_name: BITWISE_OR
```

### 1.3 file

chip.v

```
module chip(
    in, sel, clk, out
);

input  in, clk, sel;
output out;

reg    out;

core core_0 (
    .in    (in),
    .clk   (clk),
    .sel   (sel),
    .out   (out_0)
);
```

```
core core_1 (  
    .in      (out_0),  
    .clk     (clk),  
    .sel     (sel),  
    .out     (out_1)  
);  
  
core core_2 (  
    .in      (in),  
    .clk     (clk),  
    .rst_n   (1'b0),  
    .sel     (sel),  
    .out     (out_2)  
);  
  
core core_3 (  
    .in      (in),  
    .clk     (clk),  
    .rst2_n  (1'b0),  
    .sel     (sel),  
    .out     (out_2)  
);  
  
always @(posedge clk) begin  
    out <= out_0 | out_1 | out_2;  
end  
  
endmodule
```