

tile flow

1. 第一步：修改RTL源文件, tile创建port, 在顶层把这些port连起来

注：不需要使用在顶层使用create_connection去连接，这个命令有使用限制。

```
process_top_module_connections
```

```
Context: dft
```

```
Mode: setup, analysis
```

Validates and processes the content contained in a TopModuleConnections wrapper to automatically **create the DFT ports on tiled modules** and **connect them at the chip level**.

2. tile内部进行dft flow

```
mbist mbisr ijtag edt ssn occ ...
```