1. icl

2. extract_icl

- 有时候代码是直接使用ijtag spec生成来的，这种工具在生成代码的时候就会生成icl
- 有时候代码是调用多个现在模块拼接而成的，这种因为是手工写的代码，没有完整的icl需要extract_icl出完整的icl
- 有时候工具直接生成整个代码，形成一个框架或模板，后期手工又往里面加了些代码(比如可能加几级pipe等)，这种也需要重新extract_icl出完整的icl

2.1 SSN datapath

对于重新extract_icl的情况，可以先把小模块的icl读起来，读进完整的filelist 尝试extract_icl

只要icl提取出来了，就可以使用这个环境生成test case的环境。

建议为每个ssn data path都手动设置类似以下部分内容，避免重新调取icl时报错。

```
add_icl_ssn_datapaths 2
set_icl_ssn_datapath_ports -name 2 \
    -clock_inputs P_T8 -bus_data_inputs {P_T9 P_T10} -bus_data_outputs {P_T1
P_T0}
```

下面是带有ijtag和ssn重新extract_icl的例子：

1.run_ssh_edt_occ_insertion

```
#! /bin/sh
#\
exec tessent -shell -log logfiles/$0.log -replace -dofile "$0"  -
arguments ${1+"$@"}
#
# Set the context to insert DFT into RTL-level design
set_context dft -rtl -design_id rtl1
# Use dft_cell_selection that is part of the library
read_cell_library ../../../library/standard_cells/tessent/adk.tcelllib

# Set the location of the TSDB. Default is the current working
directory.
set_tsdb_output_directory ../tsdb_outdir_new

# Read the design
read_verilog  "../rtl/carrier_nco.v"
read_verilog  "../rtl/accumulator.v"
read_verilog  "../rtl/code_nco.v"
read_verilog  "../rtl/lpm_counter.v"
```

```
read_verilog  "../rtl/time_base.v"
read_verilog  "../rtl/carrier_mixer.v"
read_verilog  "../rtl/code_gen.v"
read_verilog  "../rtl/epoch_counter.v"
read_verilog  "../rtl/lpm_counter_ud.v"
read_verilog  "../rtl/lpm_shiftreg.v"
read_verilog  "../rtl/tracking_channel.v"
read_verilog
"../tsdb_outdir/dft_inserted_designs/gps_baseband_rtl1.dft_inserted_des
ign/modified_rtl_files/gps_baseband.v"
read_verilog
"../tsdb_outdir/instruments/gps_baseband_rtl1_ijtag.instrument/gps_base
band_rtl1_tessent_sib_1.v"
read_verilog
"../tsdb_outdir/instruments/gps_baseband_rtl1_ijtag.instrument/gps_base
band_rtl1_tessent_sib_2.v"
read_verilog
"../tsdb_outdir/instruments/gps_baseband_rtl1_ijtag.instrument/gps_base
band_rtl1_tessent_tdr_sri_ctrl.v"
read_verilog
"../tsdb_outdir/instruments/gps_baseband_rtl1_ssn.instrument/gps_baseba
nd_rtl1_tessent_ssn_pipe_w2_1.v"
read_verilog
"../tsdb_outdir/instruments/gps_baseband_rtl1_ssn.instrument/gps_baseba
nd_rtl1_tessent_ssn_scan_host_1.v"
read_verilog
"../tsdb_outdir/instruments/gps_baseband_rtl1_occ.instrument/gps_baseba
nd_rtl1_tessent_occ.v"
read_verilog
"../tsdb_outdir/instruments/gps_baseband_rtl1_edt.instrument/gps_baseba
nd_rtl1_tessent_edt_c1_int.v"
read_verilog
"../tsdb_outdir/instruments/gps_baseband_rtl1_edt.instrument/gps_baseba
nd_rtl1_tessent_edt_c1_ext.v"
read_verilog
"../tsdb_outdir/instruments/gps_baseband_rtl1_edt.instrument/gps_baseba
nd_rtl1_tessent_edt_c1_int_tdr.v"
read_verilog
"../tsdb_outdir/instruments/gps_baseband_rtl1_edt.instrument/gps_baseba
nd_rtl1_tessent_edt_c1_ext_tdr.v"
read_verilog
"../tsdb_outdir/instruments/gps_baseband_rtl1_edt.instrument/gps_baseba
nd_rtl1_edt_channel_out_mux_4x1_1.v"

read_verilog ./mpu.v


read_icl
../tsdb_outdir/instruments/gps_baseband_rtl1_occ.instrument/gps_baseban
d_rtl1_tessent_occ.icl
read_icl
```

```
../tsdb_outdir/instruments/gps_baseband_rtl1_ssn.instrument/gps_baseban
d_rtl1_tessent_ssn_pipe_w2_1.icl
read_icl
../tsdb_outdir/instruments/gps_baseband_rtl1_ssn.instrument/gps_baseban
d_rtl1_tessent_ssn_scan_host_1.icl
read_icl
../tsdb_outdir/instruments/gps_baseband_rtl1_ijtag.instrument/gps_baseb
and_rtl1_tessent_tdr_sri_ctrl.icl
read_icl
../tsdb_outdir/instruments/gps_baseband_rtl1_ijtag.instrument/gps_baseb
and_rtl1_tessent_sib_1.icl
read_icl
../tsdb_outdir/instruments/gps_baseband_rtl1_ijtag.instrument/gps_baseb
and_rtl1_tessent_sib_2.icl
read_icl
../tsdb_outdir/instruments/gps_baseband_rtl1_edt.instrument/gps_baseban
d_rtl1_tessent_edt_c1_int.icl
read_icl
../tsdb_outdir/instruments/gps_baseband_rtl1_edt.instrument/gps_baseban
d_rtl1_tessent_edt_c1_ext.icl
read_icl
../tsdb_outdir/instruments/gps_baseband_rtl1_edt.instrument/gps_baseban
d_rtl1_tessent_edt_c1_int_tdr.icl
read_icl
../tsdb_outdir/instruments/gps_baseband_rtl1_edt.instrument/gps_baseban
d_rtl1_tessent_edt_c1_ext_tdr.icl

read_core_descriptions
../tsdb_outdir/instruments/gps_baseband_rtl1_ssn.instrument/gps_baseban
d_rtl1_tessent_ssn_scan_host_1.tcd

#set_current_design gps_baseband
set_current_design mpu

# Set the design level as physical_block
#set_design_level physical_block
set_design_level chip

add_icl_ssn_datapaths 2
#set_icl_ssn_datapath_ports -name 1 \
    -clock_inputs P_T8 -bus_data_inputs {P_T10 P_T9} -bus_data_outputs
{P_T0 P_T1}
set_icl_ssn_datapath_ports -name 2 \
    -clock_inputs P_T8 -bus_data_inputs {P_T9 P_T10} -bus_data_outputs
{P_T1 P_T0}


check_design_rules

extract_icl
```

```
get_icl_ssn_datapath_list
get_icl_ssn_datapath_ports -name 2



# Generate patterns. Use the variable to update it if needed.
set spec [create_pattern_specification]

# Report the pattern configuration wrappers created
report_config_data $spec

# Validate pattern specification
process_pattern_specification

# Run Simulation
set_simulation_library_sources -v
../../../library/standard_cells/verilog/adk.v
#run_testbench_simulations
run_testbench_simulations -simulator vcs \
    -compilation_options "+define+debussy" \
    -simulator_options "-debug_access+all -debug_region=cell+lib -kdb -
lca"

check_testbench_simulations -report_status

exit
```

2.2 多scaninterface情况

```
INSERTION> get_icl_scan_interface_list
tap
INSERTION> get_icl_scan_interface_port_list -name tap
TCK TDI TDO TMS TRST


set_current_design tap1
add_icl_scan_interfaces {TAP Internal}
set_icl_scan_interface_ports -name TAP -ports {tck tdi tdo tms trst}
set_icl_scan_interface_ports -name Internal -ports {tdrEn1 fromTdr1 ce se
ue}
```

22.4版本会有切current_design之后，抽带SecondaryEBScanInterface情况下抽取不成功的问题，之后版本没有这个问题。

3. ICL trace

```
get_icl_fanins
get_icl_fanouts
```

用这两个命令可以trace一下icl的path结构。这个对如果让自己来理解ICL结构可能会方便一点。