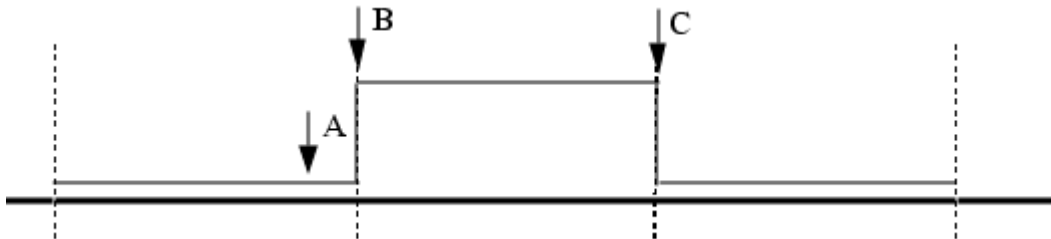


# clock

## 1. LE TE

A for clock-off, B for leading edge, and C for trailing edge events



## 2. cmd

```
add_clocks PLL_1/pll_clock_0 -reference REF_CLK -freq_multiplier 16
add_clock REF_CLK -period 48ns
add_clock INCLK -period 10ns
```

## 3. 注意项

要注意async clock 与 sync clock的区别，定义不同。

## 4. 同步时钟

```
add_clocks 0 shift_clock
```

## 5. 异步时钟

```
add_clocks REF_CLK -period 20ns
```

## 6. generated时钟

```
add_clocks PLL_1/pll_clock_0 pin -reference REF_CLK -freq_multiplier 16 -freq_divider 5
```