pt

PrimeTime 2019 Workshop Lab & Student Lab guide http://bbs.eetop.cn/thread-916544-1-1.html (出处: EETOP 创芯网论坛 (原名：电子顶级开发网))

1. report_timing

```
string report_timing
   [-from from_list
      | -rise_from rise_from_list
      | -fall_from fall_from_list]
   [-to to_list
      | -rise_to rise_to_list
      | -fall_to fall_to_list]
   [-through through_list]
   [-rise_through rise_through_list]
   [-fall_through fall_through_list]
   [-exclude exclude_list
      | -rise_exclude rise_exclude_list
      | -fall_exclude fall_exclude_list]
   [-delay_type delay_type]    #min(hold), max(setup)
   [-nworst paths_per_endpoint]
   [-max_paths max_path_count]
   [-group group_name]
   [-unique_pins]
   [-slack_greater_than minimum_slack]
   [-slack_lesser_than  maximum_slack]
   [-ignore_register_feedback feedback_slack_cutoff]
   [-report_ignored_register_feedback]
   [-include_hierarchical_pins]
   [-trace_latch_borrow]
   [-trace_latch_forward]
   [-pba_mode none | path | exhaustive]
   [-start_end_type from_to_type]
   [-normalized_slack]
   [-start_end_pair]
   [-cover_design]
   [-cover_through through_list]
   [-dont_merge_duplicates]
   [-pre_commands  pre_command_string]
   [-post_commands post_command_string]
   [-path_type format]    #full, full_clock, full_clock_expanded
   [-input_pins]
   [-nets]
   [-nosplit]
   [-transition_time]
   [-capacitance]
```

```
   [-significant_digits digits]
   [-crosstalk_delta]
   [-derate]
   [-variation]
   [-exceptions dominant | overridden | all]
   [-voltage]
   [-supply_net_group]
   [-physical]
   [-sort_by group | slack]
   [-tag_paths_filtered_by_pba tag_name]
   [path_collection]



加上-exceptions all可以报出unconstrained path
这样可以用一些special check,去检查这种异步路径的走线时延，比如用来检查FIFO

The unconstrained paths and their reason is reported for all three options
if
timing_report_unconstrained_paths variable is set to true, otherwise
unconstrained paths will not be
reported.



set_app_var timing_report_unconstrained_paths true
```

2. report_clock

```
status report_clock
   [-attributes]
   [-skew]
   [-groups]
   [-map]
   [-map_of instance_list]
   [-cells hierarchical_cell_list]
   [-include internal | virtual]
   [-exclusivity]
   [-nosplit]
   [clock_names]


report_clock -exclusivity -groups可以报出设置了哪些clock group 是通
过set_clock_groups命令。
```

3. set_clock_groups

```
status set_clock_groups
   -group clock_list
   [-exclusive]
   [-physically_exclusive]
   [-logically_exclusive]
   [-asynchronous]
   [-allow_paths]
   [-name name]
   [-comment comment_string]


set_clock_groups -physically_exclusive -group {CLK1 CLK3} -group {CLK2 CLK4}
CLK1 & CLK3是一个group,  CLK2 & CLK4是一个group,  CLK1 CLK3 与CLK2 CLK4为不
同group(异步)
```

4. create_generated_clock

```
string create_generated_clock
   [-name clock_name]
   -source master_pin
   [-divide_by divide_factor | -multiply_by multiply_factor |
    -edges edge_list ]
   [-combinational]
   [-duty_cycle percent]
   [-invert]
   [-preinvert]
   [-edge_shift edge_shift_list]
   [-add]
   [-master_clock clock]
   [-pll_output output_pin]
   [-pll_feedback feedback_pin]
   [-comment comment_string]
   source_objects


如果gen clk设置得不对的话，会导致其定义点定义不上时钟，并且之后的fanout也不会有时钟，这
点有注意。
一般在upadate timing的时候会报gen clk不能expand这时候就要去检查下gen clk是否设置正
确。


而且generated clock定义点如果原来有多个clock sources的话,
需要对每个clock sources都给定义generated clock，而且还要设置好相应的clock group
定义不全的话，会导致后续否则与相应source点之间没有timing path 可能会有timing风险。
```

5. set_sense

```
status set_sense
   [-type clock | data]
   [-non_unate]
   [-rise]
   [-fall]
   [-clock_fall]
   [-clock_rise]
   [-primary]
   [-generated]
   [-positive]
   [-negative]
   [-stop_propagation]
   [-clock_leaf]
   [-pulse pulse_type]
   [-clocks clock_list]
   object_list
```

6. report_sense

```
string report_sense
   [-type clock | data]
   [-clocks clock_list]
   [-nosplit]
   object_list
```

7. report_global_slack

Displays slack of specified pins or ports.

```
string report_global_slack
   [-significant_digits digits]
   [-nosplit]
   [-min]
   [-max]
   [-rise]
   [-fall]
   port_pin_list
```