

multicycle

1. default is single cycle timing

Default Single-Cycle Timing

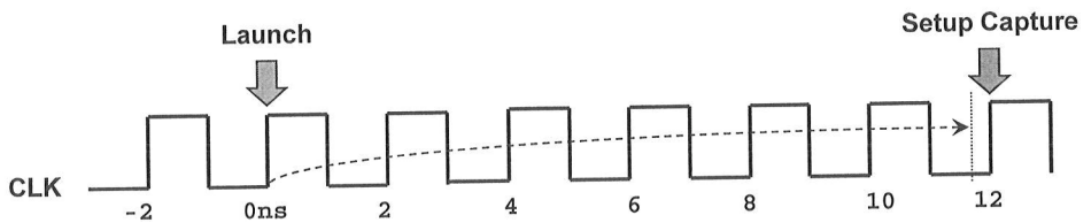
- All timing paths are constrained by **single-cycle timing**, by default, by the following implicit `set_multicycle_path` multiplier values:
 - setup = 1
 - hold = 0
- Setup capture edge occurs 1 cycle after launch edge (for single clock)
- Hold capture edge is relative to setup capture edge - occurs 1 edge before setup capture edge

- Increasing the *setup* multiplier without changing the *hold* multiplier moves both the setup and hold capture edges!

```
create_clock -period 2 [get_ports CLK]
set_multicycle_path -setup 1 <all paths>
set_multicycle_path -hold 0 <all paths>
```

2. multicycle setup timing

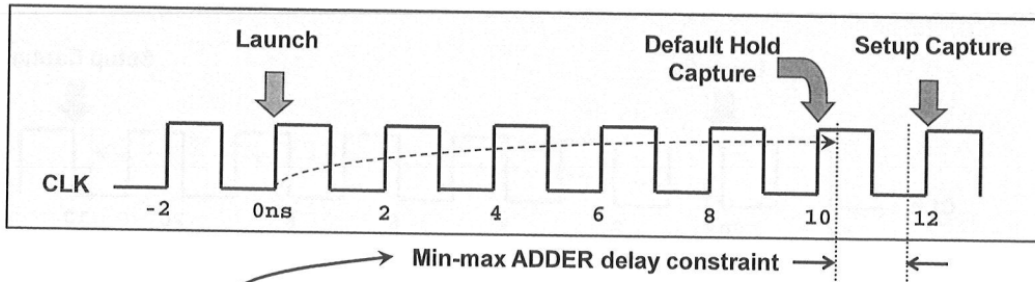
```
create_clock -period 2 [get_ports CLK]
set_multicycle_path -setup 6 -from {A_reg[*] B_reg[*]} -to C_reg[*]
```



3. multicycle hold timing

```
set_multicycle_path -setup 6 -from {A_reg[*] B_reg[*]} -to C_reg[*]
```

- The hold multiplier remains 0 → Hold capture edge is 10 ns!



- Impossible to achieve and not required (no metastability concerns)!
- Hold check can safely occur at 0ns