

===== BSCAN学习 =====

参考IEEE.Std.1149.6-2003.pdf

1. JTAG TAP FSM

{:edastudy:pasted:20231227-145930.png?nolink}}

2. tesseract bscan interface

左侧是开了ac_control选项，右侧没有开，生成出来bscan interface模块的区别：

{:edastudy:pasted:20240606-092347.png?nolink&900}}

3. AC test signal

^ tesseract tap ^ SNPS PHY信号 ^ 说明 ^ | to_bscan_ac_mode_en | bs_acmode | 表示EXTEST_PULSE or EXTEST_TRAIN有效，处于BSCAN AC测试模式 || to_bscan_ac_signal | bs_actest | 在JTAG IDLE状态，测试信号拉高[]EXTEST_PULSE模式)，测试信号按TCK周期翻转[]EXTEST_TRAIN) || to_bscan_ac_init_clock0 | bs_rx_init || | to_bscan_ac_init_clock1 || ~to_bscan_ac_init_clock0 |

{:edastudy:bscan:pasted:20250523-150523.png?nolink}}

{:edastudy:bscan:pasted:20250523-095725.png?nolink}}

ac test signal\{:edastudy:pasted:20231227-145232.png?nolink}}

```
<code> ACMODE = EXTEST_TRAIN | EXTEST_PULSE;
```

```
ac_signal = RTI & ACMODE;
```

```
bscan_select = EXTEST_decoded | INTEST_decoded | EXTEST_PULSE_decoded |
```

```
EXTEST_TRAIN_decoded | EXTEST_PRELOAD_decoded;
```

```
ac_init_clk0 = ac_init_clk_EXTEST | ac_init_clk_EXTEST_TRAIN_OR_PULSE; ac_init_clk1 = ~ ac_init_clk0;
```

```
ac_init_clk_EXTEST = SDR & bscan_select; ac_init_clk_EXTEST_TRAIN_OR_PULSE = (E1DR | E2DR) & ACMODE; </code>
```

4. Input test receivers

接收器在接收的时候分为DC Coupled和AC Coupled[]

{:edastudy:pasted:20231227-154631.png?nolink}}

所述接收器，应该在capture-DR状态时能采样到一个有效的值，如果不能采到有效值，应该会有一个initial value被采到。

{{:edastudy:pasted:20231227-154750.png?nolink}}

就如下图一样在capture-DR状态采到有效值或者initial value

{{:edastudy:pasted:20231227-154935.png?nolink}}

所以接收器在Exit1-DR或者Exit2-DR (其实就是在Update状态之前先给个initial值)的时候可以把sample register给个initial state(比如说固定为0)，接收器示范电路如下：

{{:edastudy:pasted:20231227-155250.png?nolink}}

{{:edastudy:pasted:20231227-155317.png?nolink}}

5. Output drivers

output driver不会太特殊

{{:edastudy:pasted:20231227-155806.png?nolink}}

{{:edastudy:pasted:20231227-155906.png?nolink}}

6. instruction

6.1 EXTEST_PULSE

{{:edastudy:pasted:20231227-145507.png?nolink}}

6.2 EXTEST_TRAIN

{{:edastudy:pasted:20231227-145540.png?nolink}}

7. clockdr & updatedr

`clockir = 1) ? tck : 1'b1; clockdr = 2) ? tck : 1'b1;` 在capture状态capture数据，在shift状态在shift数据。

{{:edastudy:pasted:20240122-092432.png?nolink}}

8. tessent BC cell

ref: bsda_ref.pdf

8.1 BC_1

{{:edastudy:pasted:20240122-094711.png?nolink}}

8.2 BC_2

{{:edastudy:pasted:20240122-094642.png?nolink}}

8.3 BC_2_A

{{:edastudy:pasted:20240122-094212.png?nolink}}

8.4 BC_2_A_EXT

{{:edastudy:pasted:20240122-094535.png?nolink}}

8.5 BC_2_B

{{:edastudy:pasted:20240122-094324.png?nolink}}

8.6 BC_3

{{:edastudy:pasted:20240122-094405.png?nolink}}

8.7 BC_4

{{:edastudy:pasted:20240122-094446.png?nolink}}

8.8 BC_5

{{:edastudy:pasted:20240122-094759.png?nolink}}

8.9 BC_7

{{:edastudy:pasted:20240122-094836.png?nolink}}

8.10 BC_7_LOW

{{:edastudy:pasted:20240122-094917.png?nolink}}

8.11 BC_8

{{:edastudy:pasted:20240122-094959.png?nolink}}

8.12 BC_9

{{:edastudy:pasted:20240122-095034.png?nolink}}

8.13 BC_10

{{:edastudy:pasted:20240122-095104.png?nolink}}

9. tessent AC cell

ref: bsda_ref.pdf

9.1 AC_1

{{:edastudy:pasted:20240122-095245.png?nolink}}

9.2 AC_2

{{:edastudy:pasted:20240122-095308.png?nolink}}

9.3 AC_7

{{:edastudy:pasted:20240122-095342.png?nolink}}

9.4 AC_7_LOW

{{:edastudy:pasted:20240122-095406.png?nolink}}

9.5 AC_8

{{:edastudy:pasted:20240122-095446.png?nolink}}

9.6 AC_9

{{:edastudy:pasted:20240122-095515.png?nolink}}

9.7 AC_10

{{:edastudy:pasted:20240122-095540.png?nolink}}

10. IEEE 1149.1 BSCAN BC cell

- BC_1, input cell, control cell, capture misson input
- BC_2, input cell, control cell, capture misson output
- BC_4, Observe-only input cell without control
- BC_7, BIDI双向 data cell; capture UPD/PAD input/misson output
- BC_8, BIDI双向 data cell; capture PAD output
- BC_9, self-monitor output cell; mode 4 capture PAD output, else capture mission input
- BC_10, self-monitor output cell; capture PAD output only

10.1 BC_1

mode

{{:edastudy:pasted:20240119-163524.png?nolink}}

{{:edastudy:pasted:20240119-161410.png?nolink}}

10.2 BC_2

{{:edastudy:pasted:20240119-163827.png?nolink}}

{{:edastudy:pasted:20240119-161454.png?nolink}}

10.3 BC_3

个人觉得BC_3不会使用

{{:edastudy:pasted:20240119-161524.png?nolink}}

10.4 BC_4

{{:edastudy:pasted:20240119-161555.png?nolink}}

10.5 BC_5

{{:edastudy:pasted:20240119-164010.png?nolink}}

{{:edastudy:pasted:20240119-161735.png?nolink}}

10.6 BC_7

{{:edastudy:pasted:20240119-164112.png?nolink}}

{{:edastudy:pasted:20240119-161818.png?nolink}}

10.7 BC_8

mode

{{:edastudy:pasted:20240119-163150.png?nolink}}

{{:edastudy:pasted:20240119-161856.png?nolink}}

bc_2 control + bc_8

{{:edastudy:pasted:20240119-163310.png?nolink}}

10.8 BC_9

{{:edastudy:pasted:20240119-164214.png?nolink}}

{{:edastudy:pasted:20240119-161929.png?nolink}}

10.9 BC_10

{{:edastudy:pasted:20240119-164254.png?nolink}}

{{:edastudy:pasted:20240119-161958.png?nolink}}

11. BSCAN AC cell

- AC_SelX, 控制选择AC/DC测试模式□ capture的值永远是X□即不关注capture到的值

- AC_SelU, 控制选择AC/DC测试模式 capture的值是UPD即capture到的值是上一次配置的AC/DC的选择值。
- AC_1, input cell, control cell, capture misson input
- AC_2, input cell, control cell, capture misson output
- AC_7, BIDI双向 data cell; capture UPD/PAD input/misson output
- AC_8, BIDI双向 data cell; capture PAD output
- AC_9, self-monitor output cell; mode 4 capture PAD output, else capture mission input
- AC_10, self-monitor output cell; capture PAD output only

^ ^ mode 1 ^ mode 2 ^ mode 3 ^ mode 4 ^ mode 5 ^ | EXTEST | 1 | 0 | 1 | 1 | 1 | | PRELOAD | 0 | 0 |
 1 | X | 0 | | SAMPLE | 0 | 0 | 1 | 0 | 0 | | INTEST | 0 | 1 | 0 | 0 | 1 | | RUNBIST | X | X | 0 | X | 1 | | CLAMP |
 1 | X | 1 | X | 1 | | HIGHZ | X | X | 0 | X | X | | NOTES:\ 1. EXTEST inluce EXTEST, EXTEST_PLUSE,
 EXTEST_TRAIN |||||

11.1 AC_SelX

{{:edastudy:pasted:20231227-144008.png?nolink}}

11.2 AC_SelU

{{:edastudy:pasted:20231227-144100.png?nolink}}

11.3 AC_1

{{:edastudy:pasted:20231227-144150.png?nolink}}

11.4 AC_2

{{:edastudy:pasted:20231227-144237.png?nolink}}

11.5 AC_7

{{:edastudy:pasted:20231227-144322.png?nolink}}

11.6 AC_8

{{:edastudy:pasted:20231227-144400.png?nolink}}

11.7 AC_9

{{:edastudy:pasted:20231227-144439.png?nolink}}

11.8 AC_10

{{:edastudy:pasted:20231227-144505.png?nolink}}

12. BSCAN指令

12.1 SAMPLE

只sample采样 capture pin input & output值，而不能影响其input pin到内部逻辑值和output pin到PAD的状态。

12.2 PRELOAD

主要用来更新update DR的值，这个值在后面的测试指令作用下，将会直接被驱动到output PAD脚；如果值没有初始化，将不确定输出的是什么值。

一般后面会再跟一个EXTEST指令，将PRELOAD初始化的值驱动到output PAD上。

1)

```
pstate == capture_IR) || (pstate == shift_IR
```

2)

```
pstate == capture_DR) || (pstate == shift_DR
```