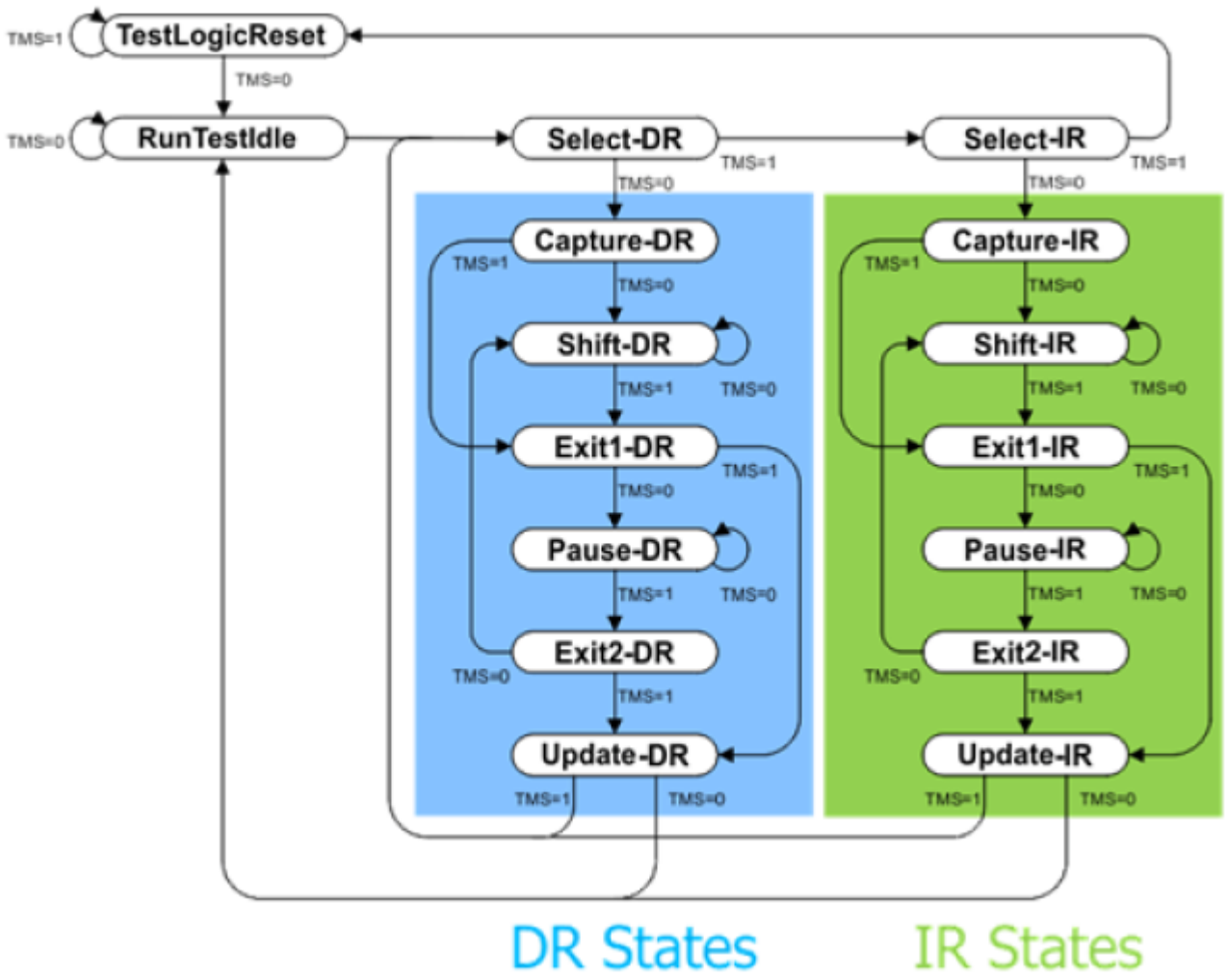
BSCAN学习

参考IEEE.Std.1149.6-2003.pdf

1. JTAG TAP FSM



2. tessent bscan interface

左侧是开了ac_control选项，右侧没有开，生成出来bscan interface模块的区别：

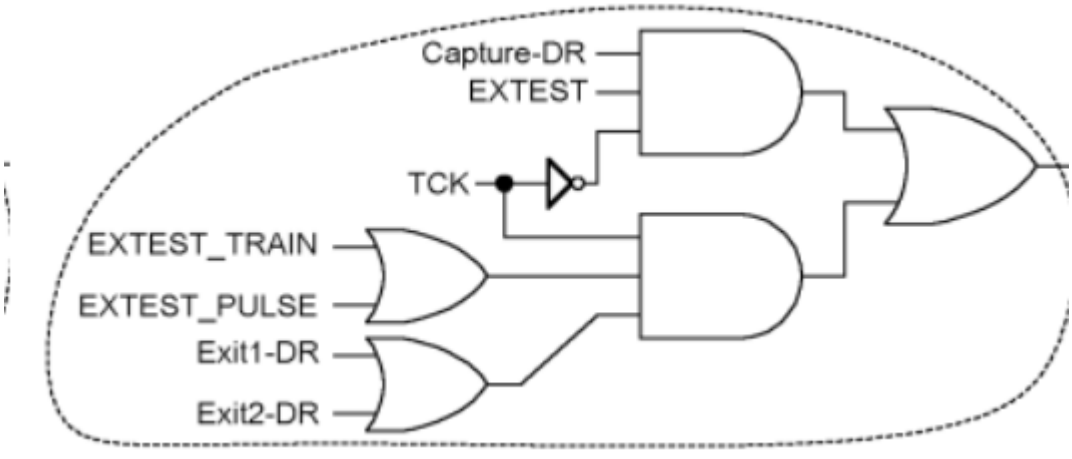
```
module chip_top_rtl1_tessent_bscan_interface (
  // from the TAP
  input  wire         ijtag_tck,
  input  wire   [3:0] state,
  input  wire         tms,
  input  wire         trst,
  input  wire         scan_in,
  input  wire         ijtag_resetn,
  input  wire         bscan_select,
  input  wire         ijtag_shift_en,
  input  wire         ijtag_update_en,
  input  wire         ijtag_capture_en,
  input  wire         force_disable,
  input  wire         select_jtag_input,
  input  wire         select_jtag_output,
  input  wire         extest_pulse,
  input  wire         extest_train,
  input  wire         output_pad_disable,
  input  wire         bscan_clamp_enable,
  // for the logic test
  input  wire         ltest_si,
  input  wire         ltest_se,
  input  wire         ltest_shift_capture_clock,
+-- 15 lines: input  wire         ltest_en,----------
  output wire         to_bscan_select,
  output wire         to_bscan_shift_en,
  output wire         to_bscan_update_en,
  output wire         to_bscan_capture_shift_clock,
  output wire         to_bscan_update_clock,
  output wire         to_bscan_capture_en,
  output wire         to_bscan_ac_mode_en,
  output wire         to_bscan_ac_init_clock0,
  output wire         to_bscan_ac_init_clock1,
  output wire         to_bscan_ac_signal,
  output wire         to_bscan_select_jtag_input,
  output wire         to_bscan_select_jtag_output,
  output wire         to_bscan_pad_sel,
  output wire         to_bscan_scan_in
);
```

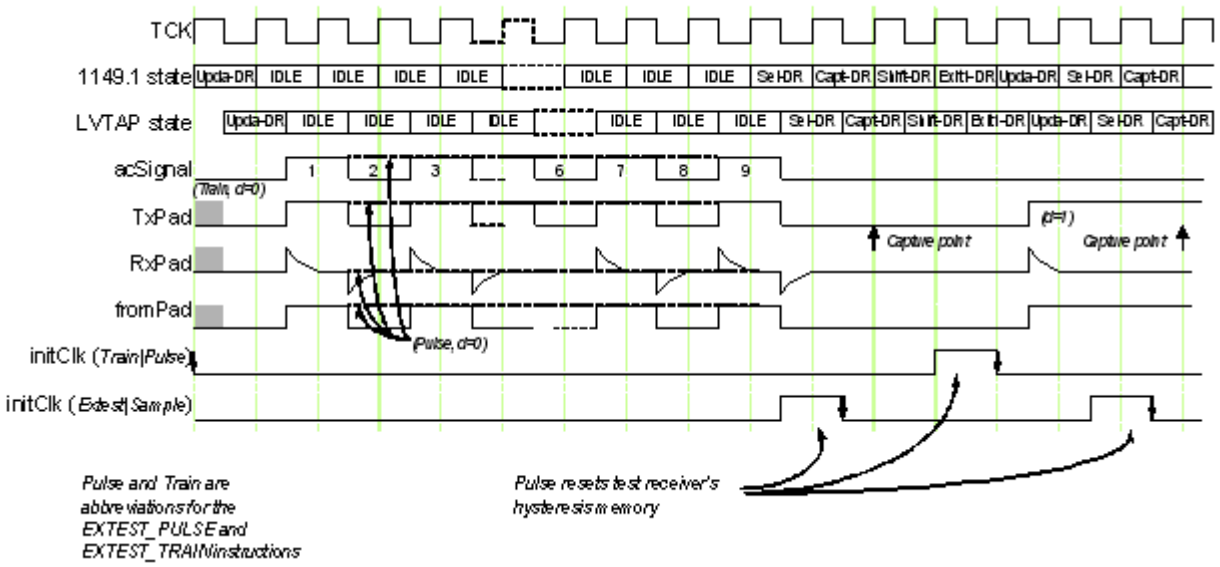
```
module chip_top_rtl1_tessent_bscan_interface (
  // from the TAP
  input  wire         ijtag_tck,
  input  wire         scan_in,
  input  wire         bscan_select,
  input  wire         ijtag_shift_en,
  input  wire         ijtag_update_en,
  input  wire         ijtag_capture_en,
  input  wire         force_disable,
  input  wire         select_jtag_input,
  input  wire         select_jtag_output,
  input  wire         output_pad_disable,
  input  wire         bscan_clamp_enable,
  // for the logic test
  input  wire         ltest_si,
  input  wire         ltest_se,
  input  wire         ltest_shift_capture_clock,
+-- 15 lines: input  wire         ltest_en,----------
  output wire         to_bscan_select,
  output wire         to_bscan_shift_en,
  output wire         to_bscan_update_en,
  output wire         to_bscan_capture_shift_clock,
  output wire         to_bscan_update_clock,
  output wire         to_bscan_capture_en,
  output wire         to_bscan_select_jtag_input,
  output wire         to_bscan_select_jtag_output,
  output wire         to_bscan_pad_sel,
  output wire         to_bscan_scan_in
);
```

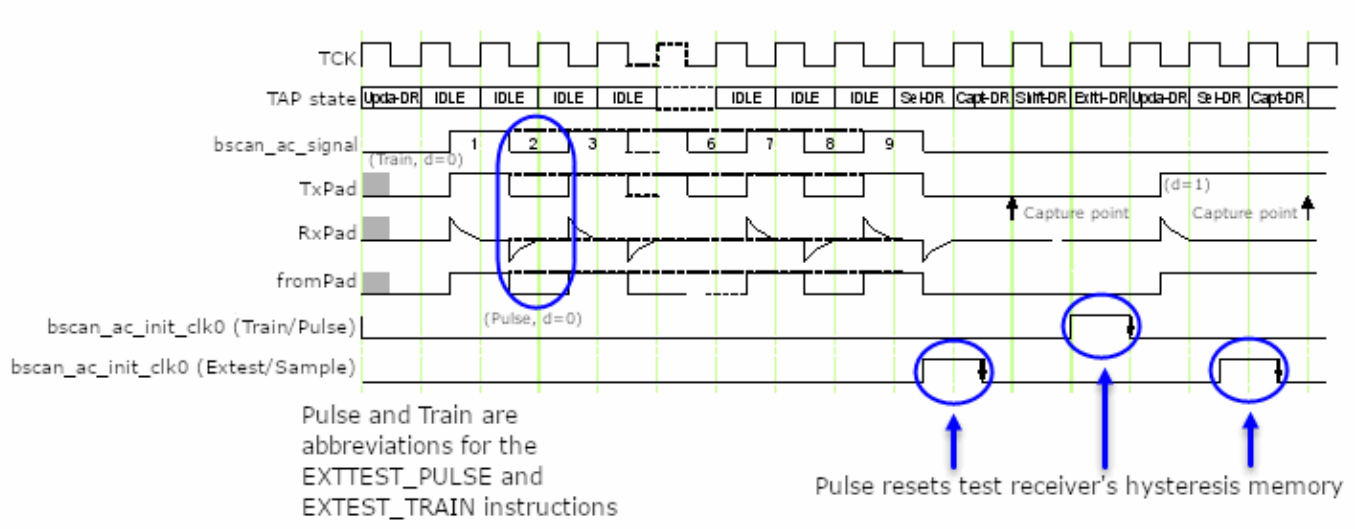
3. AC test signal

tessent tap	SNPS PHY信号	说明
to_bscan_ac_mode_en	bs_acmode	表示EXTEST_PULSE or EXTEST_TRAIN有效，处于BSCAN AC测试模式
to_bscan_ac_signal	bs_actest	在JTAG IDLE状态，测试信号拉高（EXTEST_PULSE模式）,测试信号按TCK周期翻转（EXTEST_TRAIN)
to_bscan_ac_init_clock0	bs_rx_init	
to_bscan_ac_init_clock1		~to_bscan_ac_init_clock0

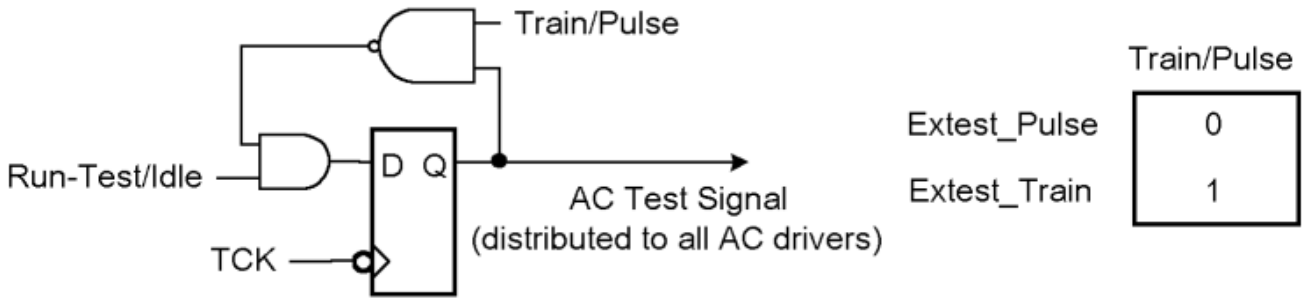
initclk







ac test signal, 只在RTI模式下数据才有效 pulse or train

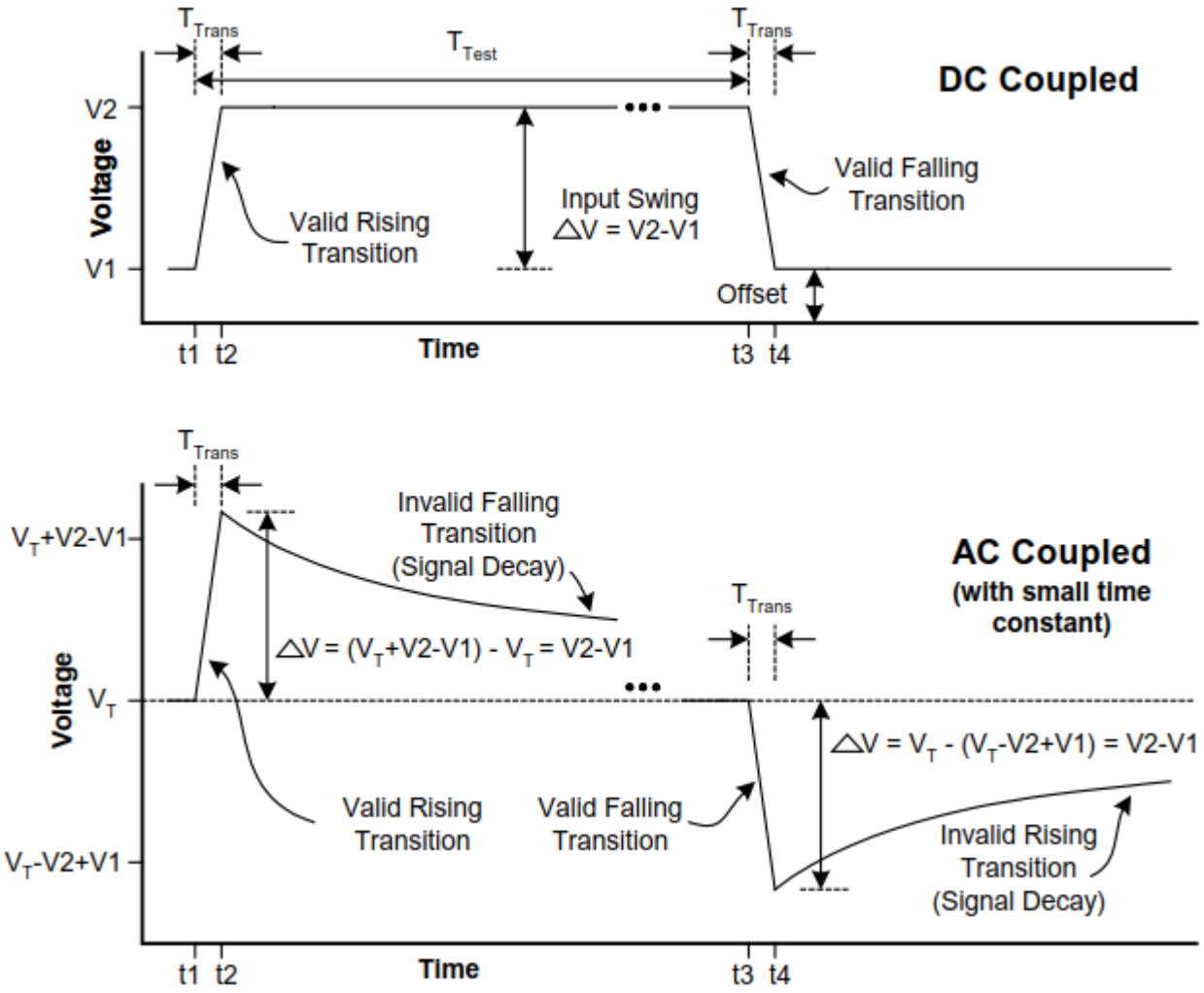



```
ACMODE = EXTEST_TRAIN | EXTEST_PULSE;

ac_signal = RTI & ACMODE;

bscan_select = EXTEST_decoded | INTEST_decoded | EXTEST_PULSE_decoded |
               EXTEST_TRAIN_decoded | EXTEST_PRELOAD_decoded;

ac_init_clk0 = ac_init_clk_EXTEST | ac_init_clk_EXTEST_TRAIN_OR_PULSE;
ac_init_clk1 = ~ ac_init_clk0;
```

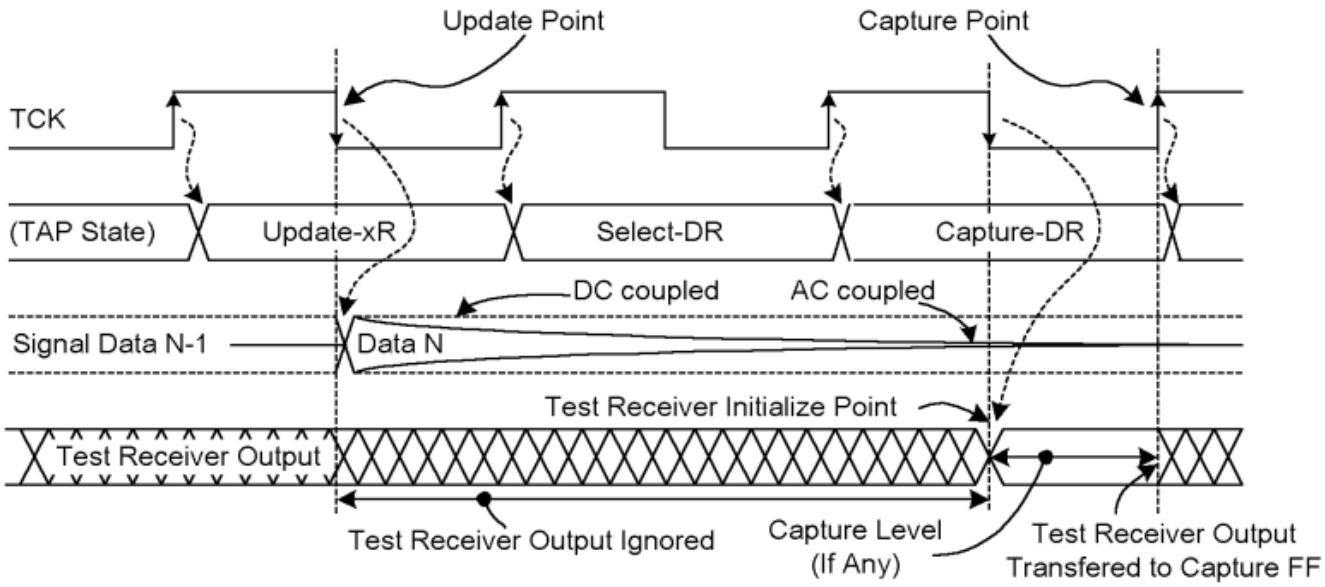
```
ac_init_clk_EXTEST = SDR & bscan_select;
ac_init_clk_EXTEST_TRAIN_OR_PULSE = (E1DR | E2DR) & ACMODE;
```

4. Input test receivers

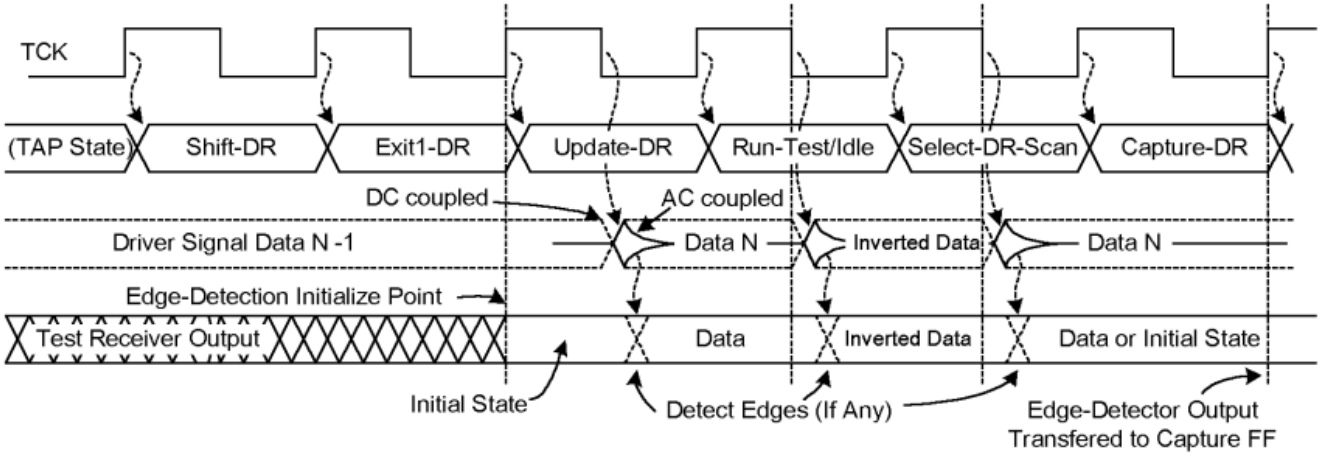
接收器在接收的时候分为DC Coupled和AC Coupled



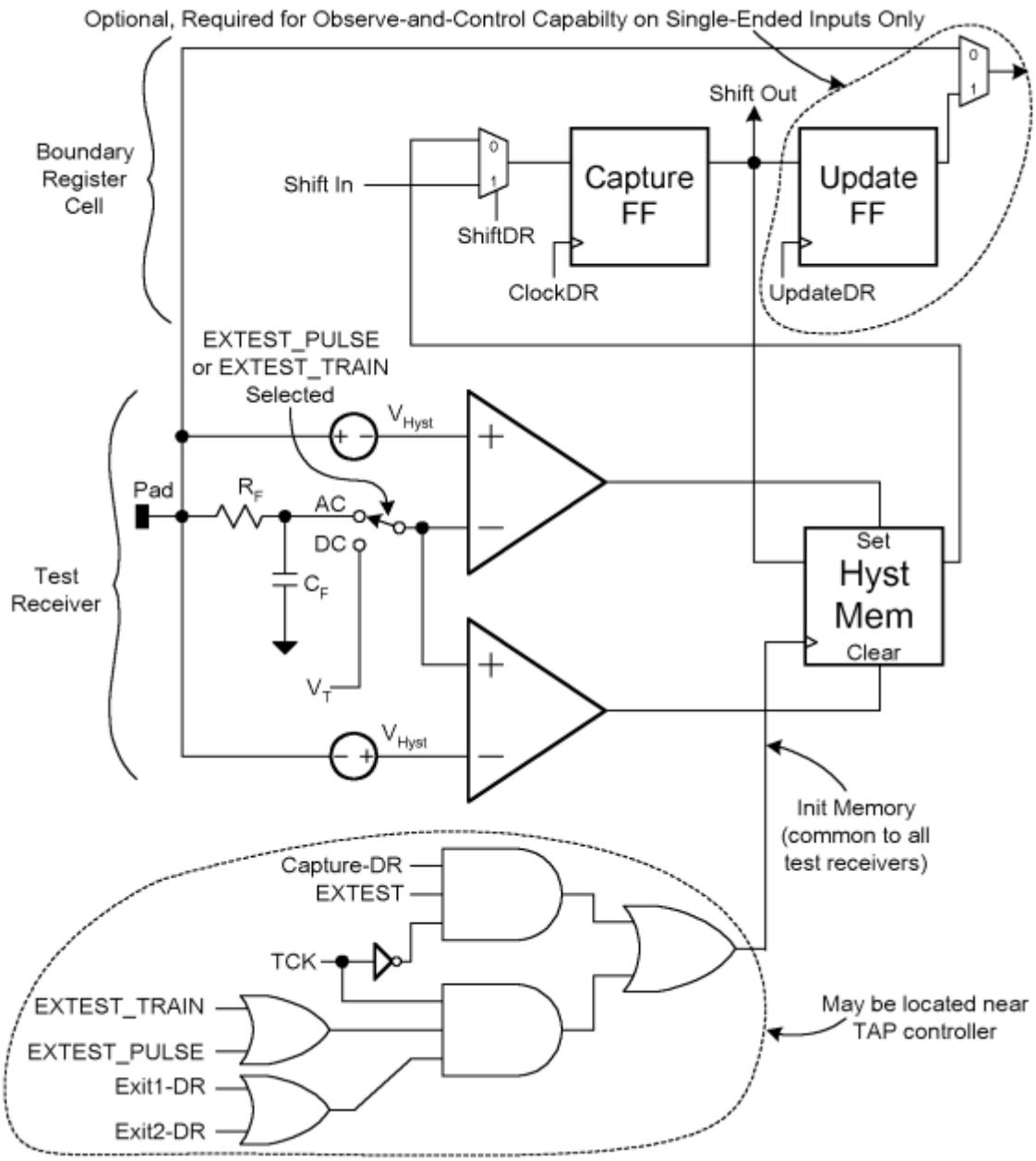
EXTEST测试时，在capture-DR状态TCK下降沿，接收器给一个初始值

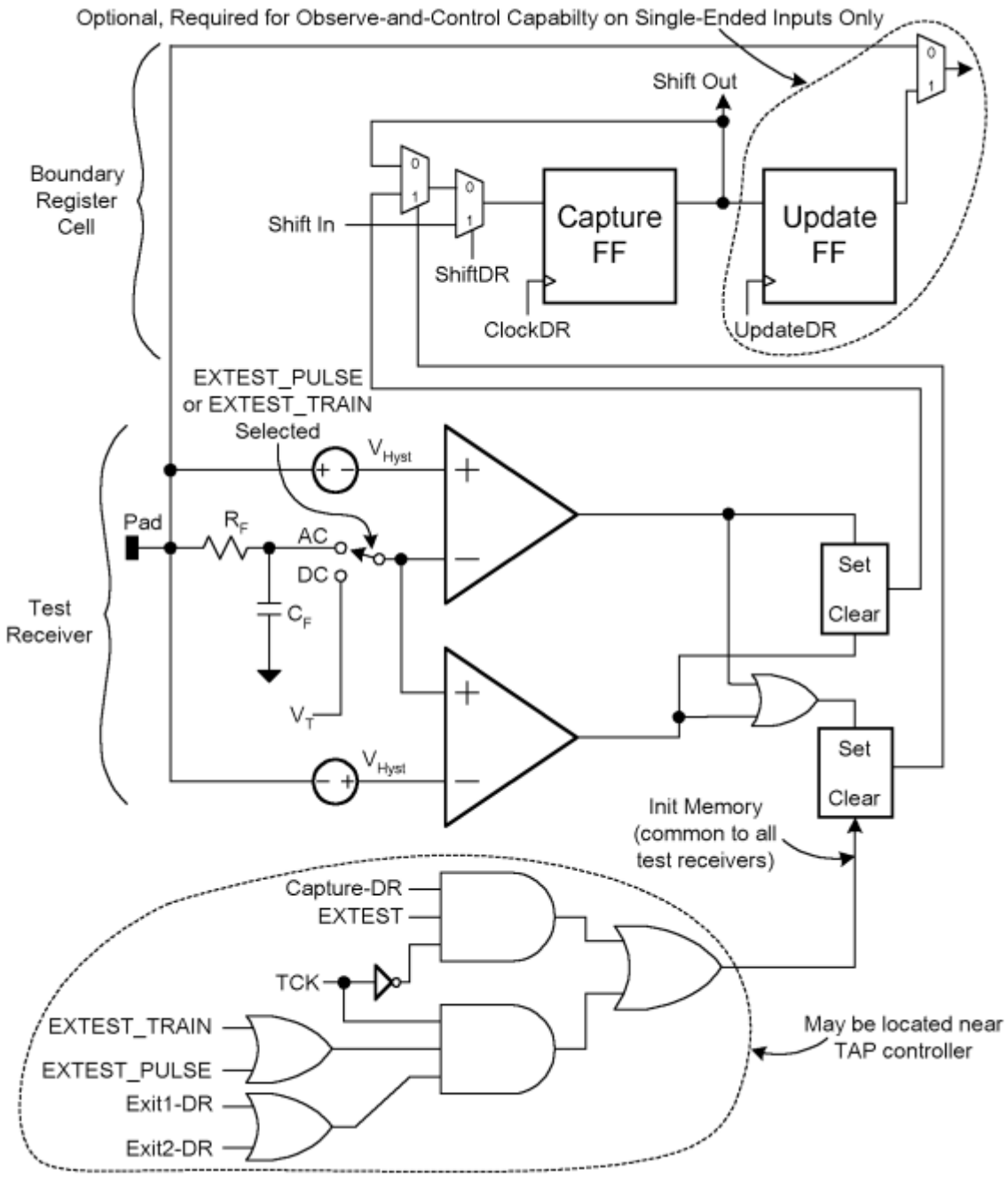


AC EXTEST测试时，在TCK上升沿□updata DR状态时前，接收器给一个初始值



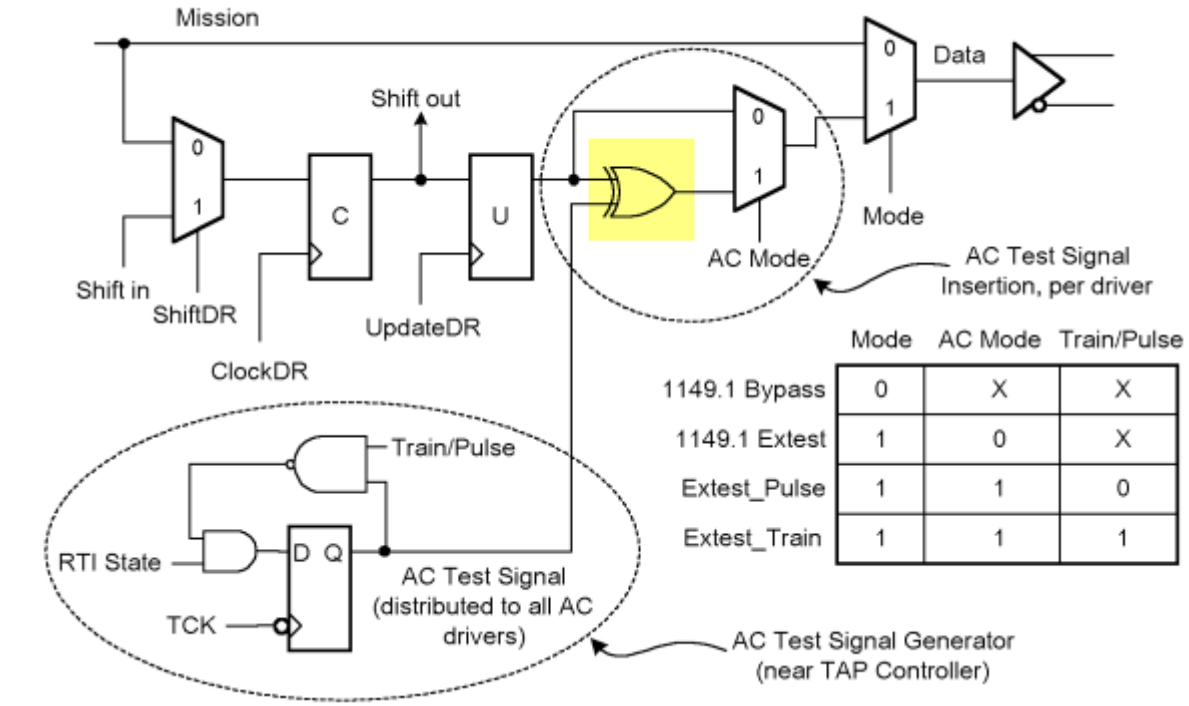
接收器示范电路如下：


Optional, Required for Observe-and-Control Capabilty on Single-Ended Inputs Only
Boundary Register Cell
Shift In
ShiftDR
Capture FF
ClockDR
Shift Out
Update FF
UpdateDR
EXTEST_PULSE or EXTEST_TRAIN Selected
Test Receiver
Pad
R_F
AC
DC
C_F
V_T
V_{Hyst}
V_{Hyst}
Set Hyst Mem Clear
Init Memory (common to all test receivers)
Capture-DR
EXTEST
TCK
EXTEST_TRAIN
EXTEST_PULSE
Exit1-DR
Exit2-DR
May be located near TAP controller

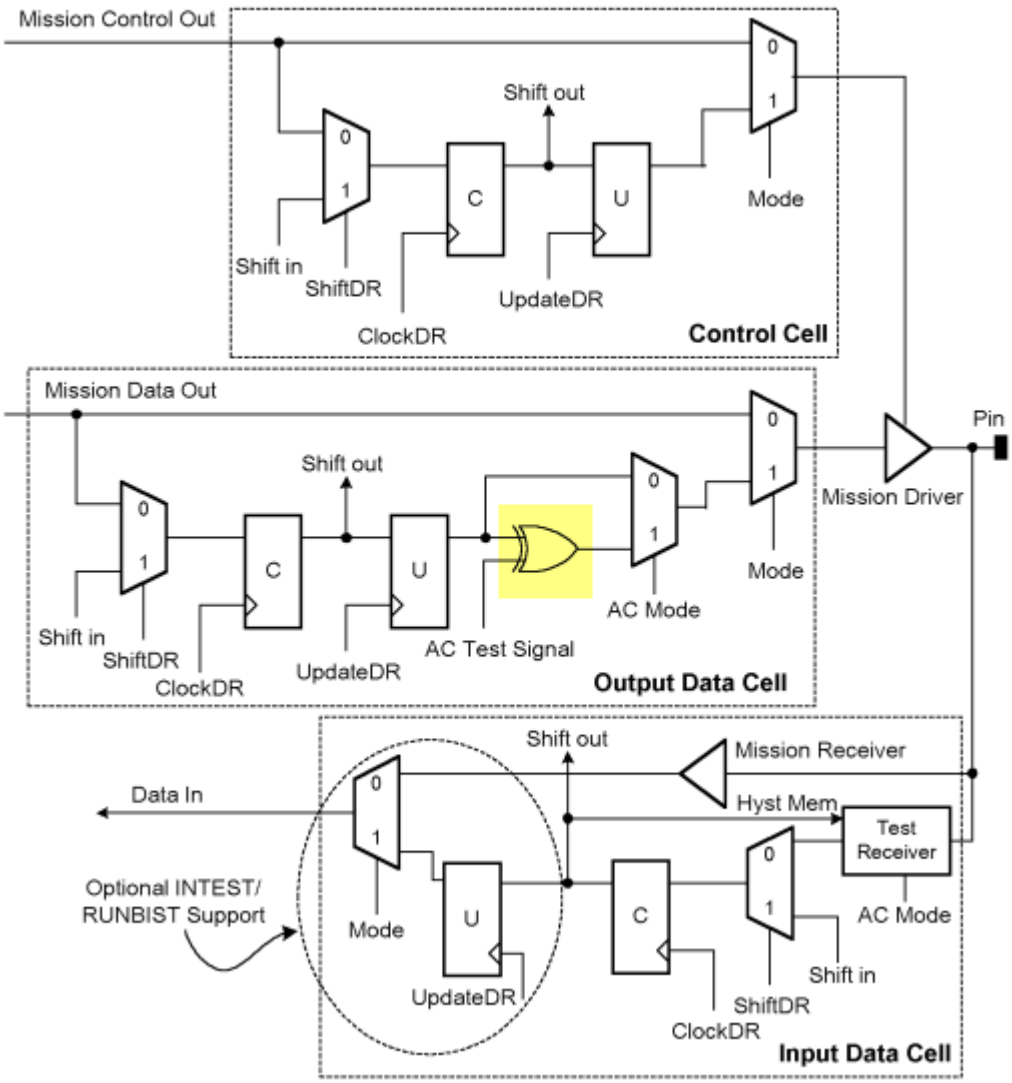


5. Output drivers

output driver不会太特殊

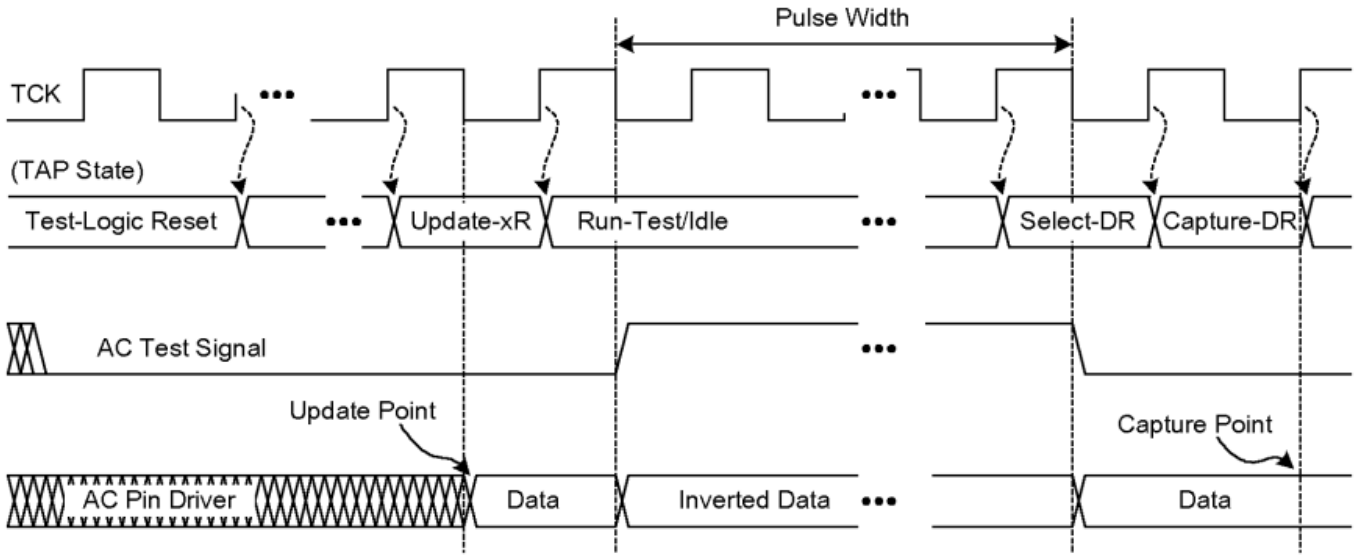


Mode	AC Mode	Train/Pulse
1149.1 Bypass	0	X	X
1149.1 Extest	1	0	X
Extest_Pulse	1	1	0
Extest_Train	1	1	1

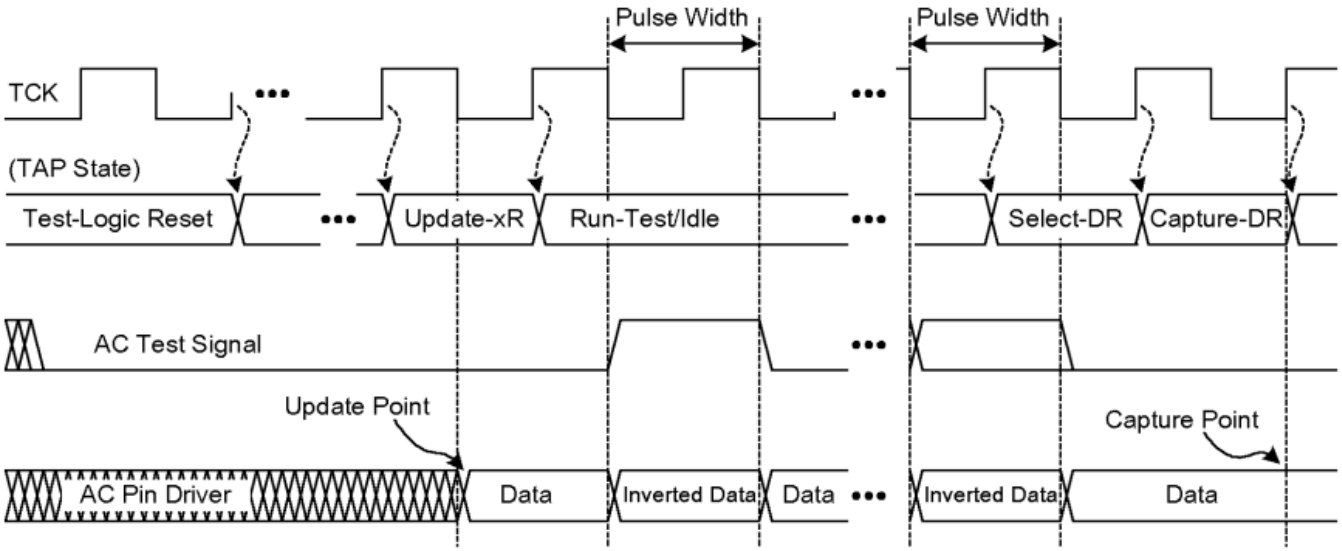


6. instruction

6.1 EXTEST_PULSE



6.2 EXTEST_TRAIN



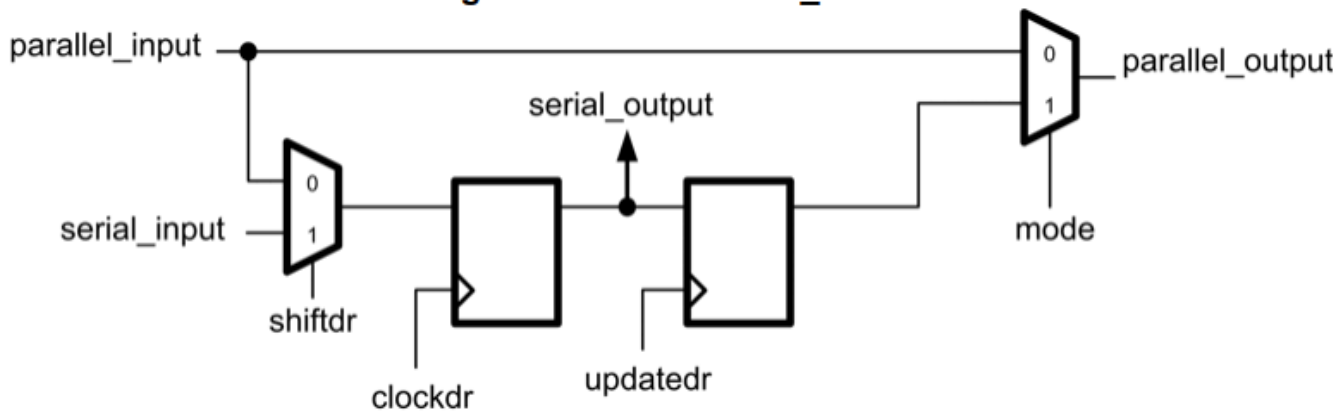
7. clockdr & updatedr

```
clockir = ((pstate == capture_IR) || (pstate == shift_IR)) ? tck : 1'b1;
clockdr = ((pstate == capture_DR) || (pstate == shift_DR)) ? tck : 1'b1;
```

在capture状态capture数据，在shift状态□shift数据。

BC_1 Cell

Figure 4-1. Generic BC_1 Cell

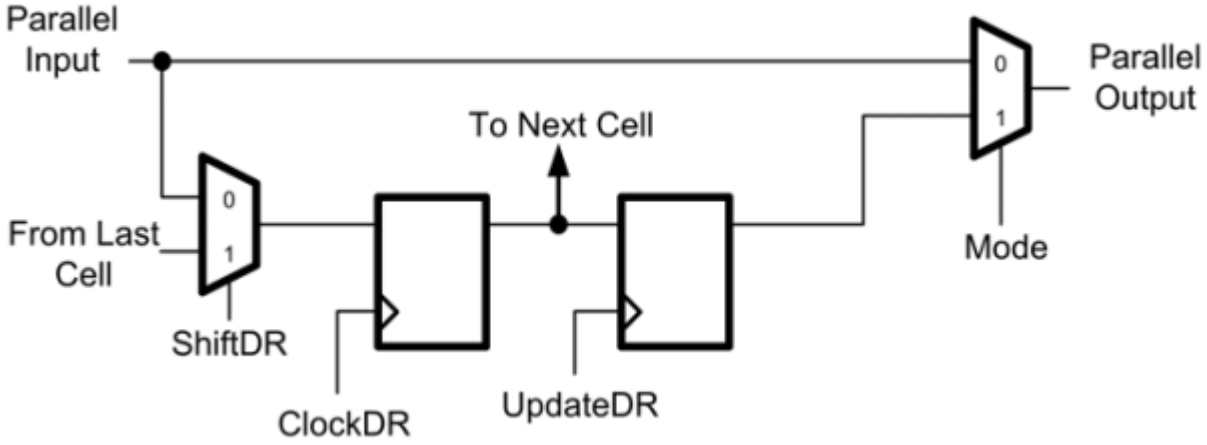


8. tessent BC cell

ref: bsda_ref.pdf

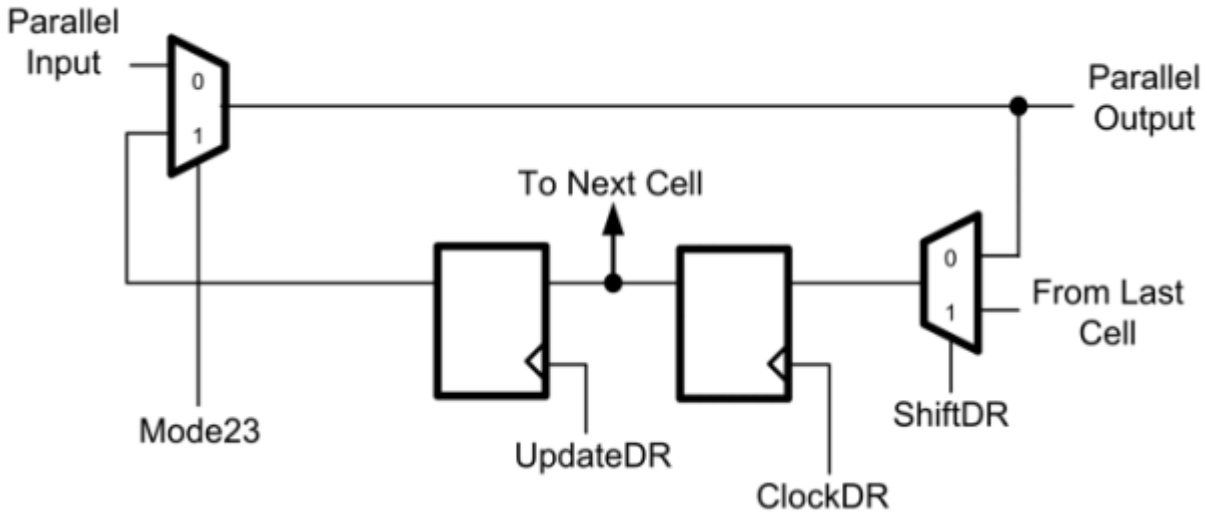
8.1 BC_1

Figure A-1. BC_1 Type Cell



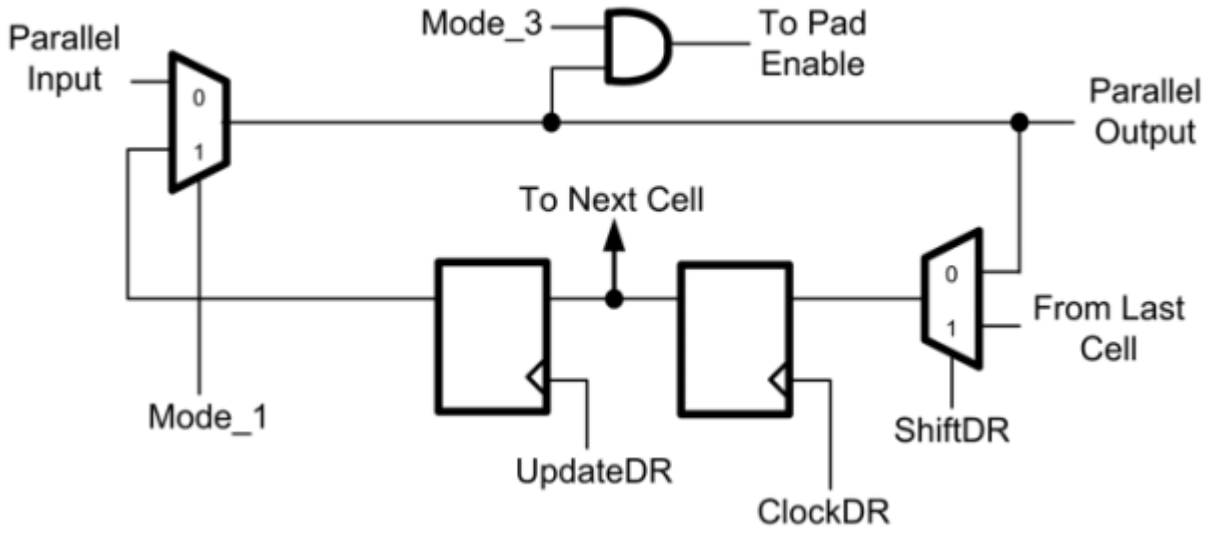
8.2 BC_2

Figure A-2. BC_2 Type Cell



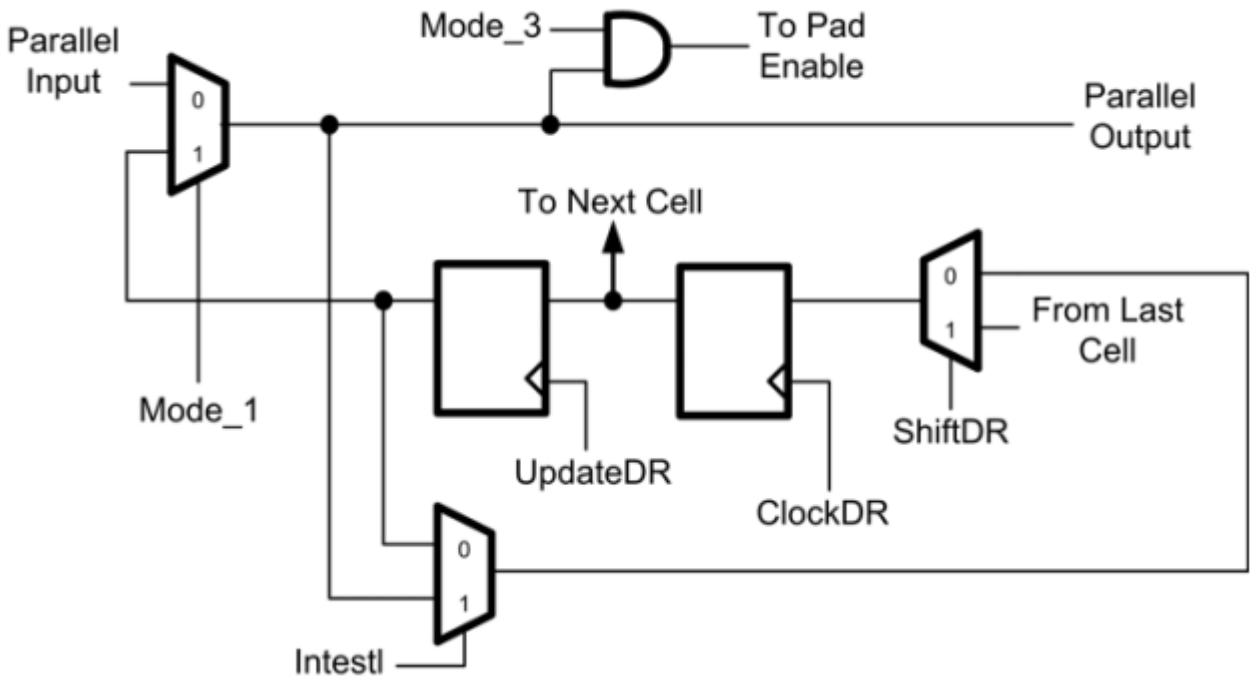
8.3 BC_2_A

Figure A-3. BC_2_A Type Cell



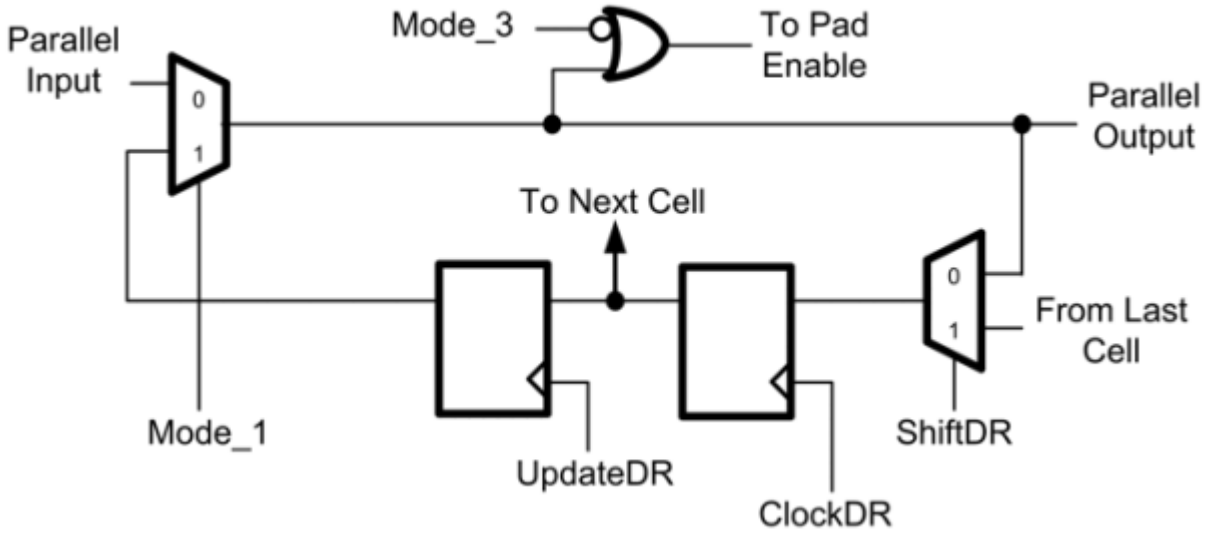
8.4 BC_2_A_EXT

Figure A-4. BC_2_A_EXT Type Cell



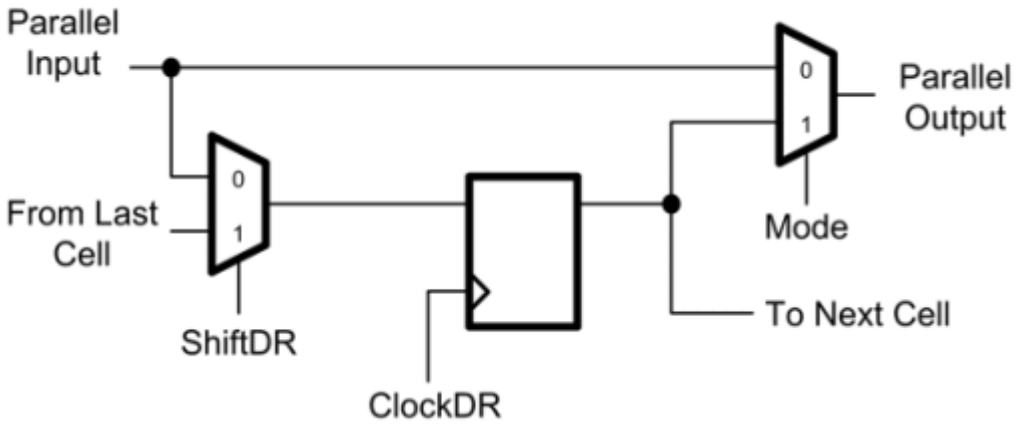
8.5 BC_2_B

Figure A-5. BC_2_B Type Cell



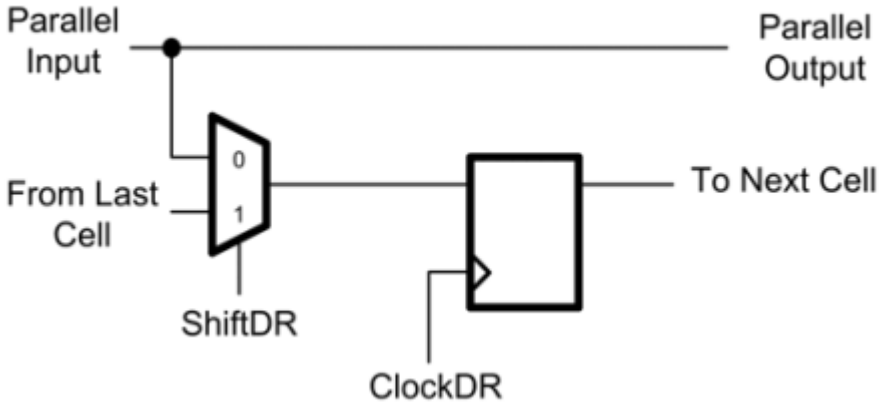
8.6 BC_3

Figure A-6. BC_3 Type Cell



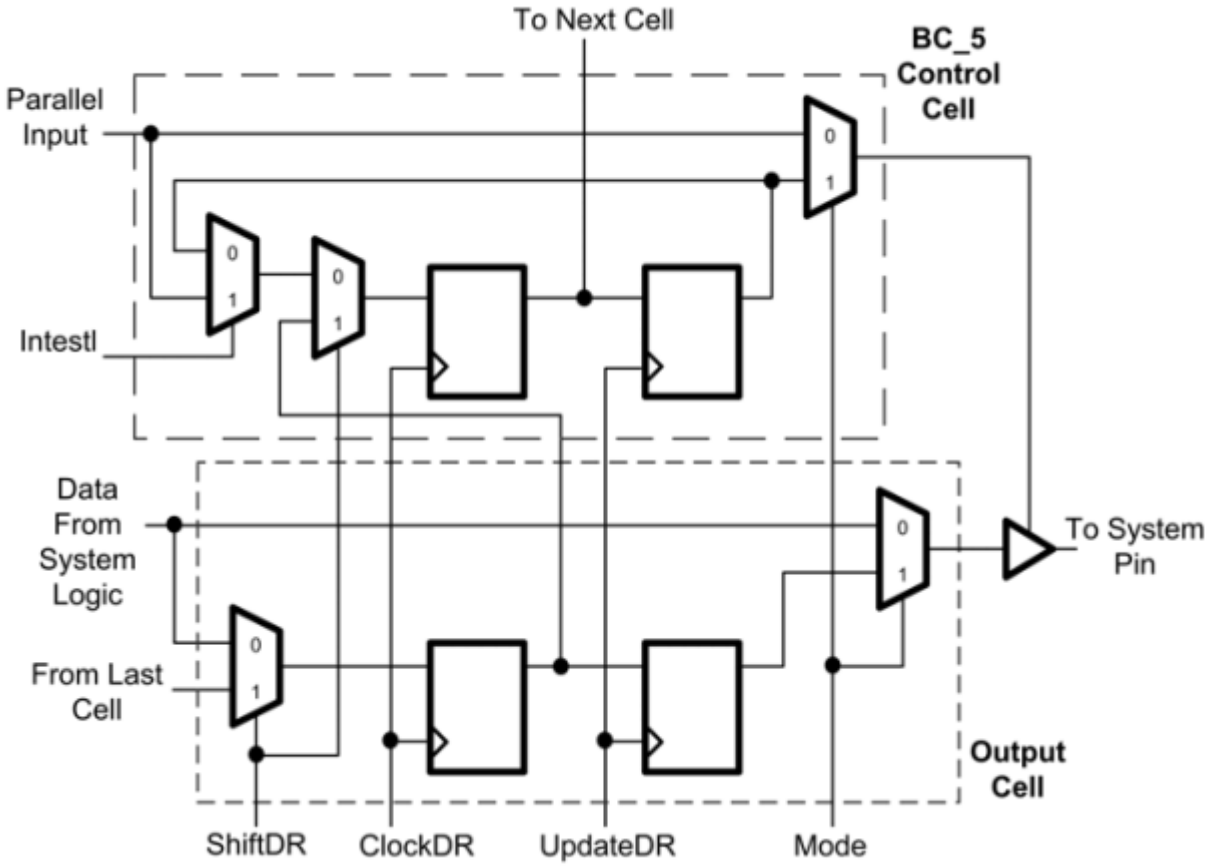
8.7 BC_4

Figure A-7. BC_4 Type Cell



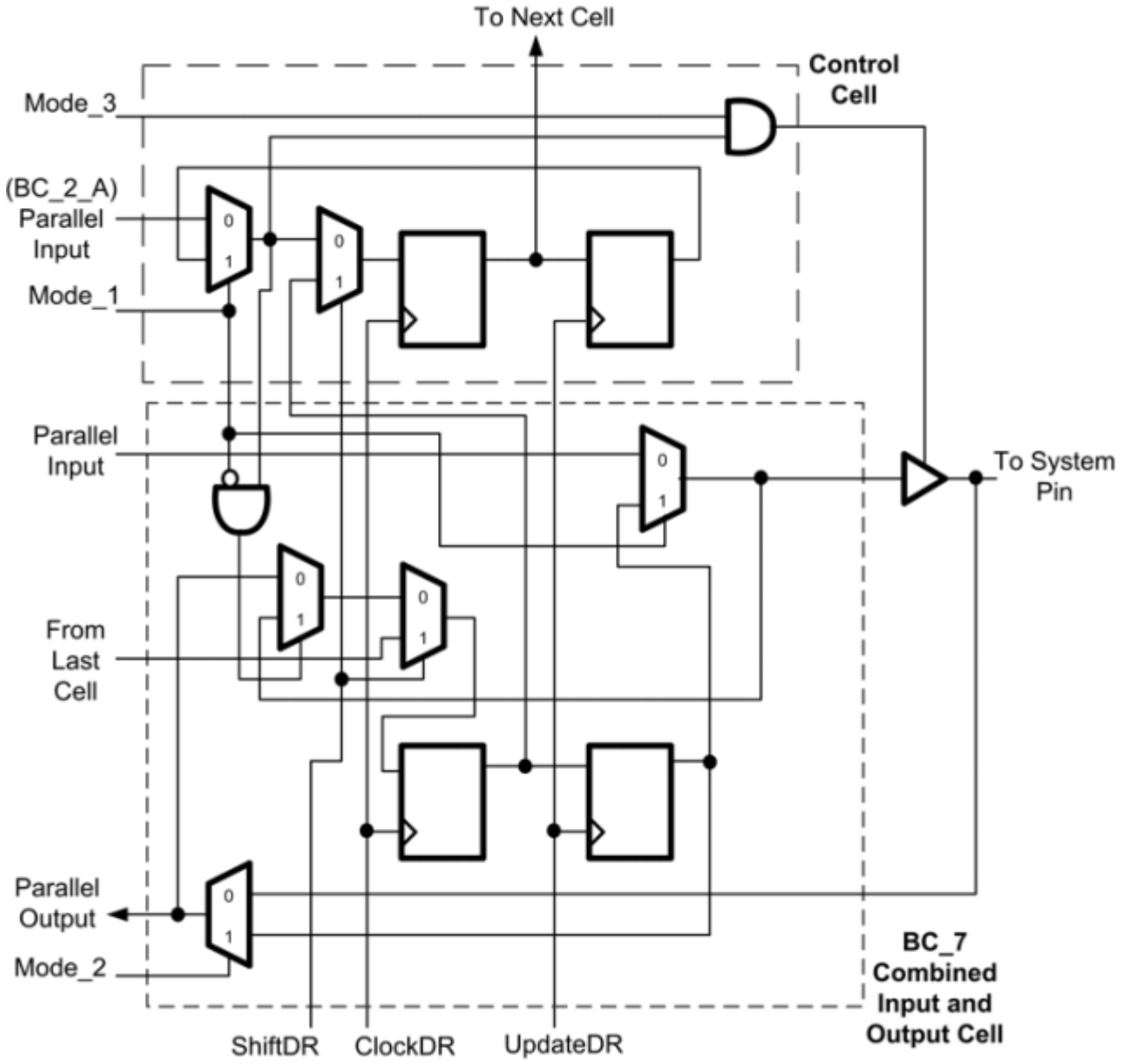
8.8 BC_5

Figure A-8. BC_5 Type Cell Shown with BC_1 Output Cell



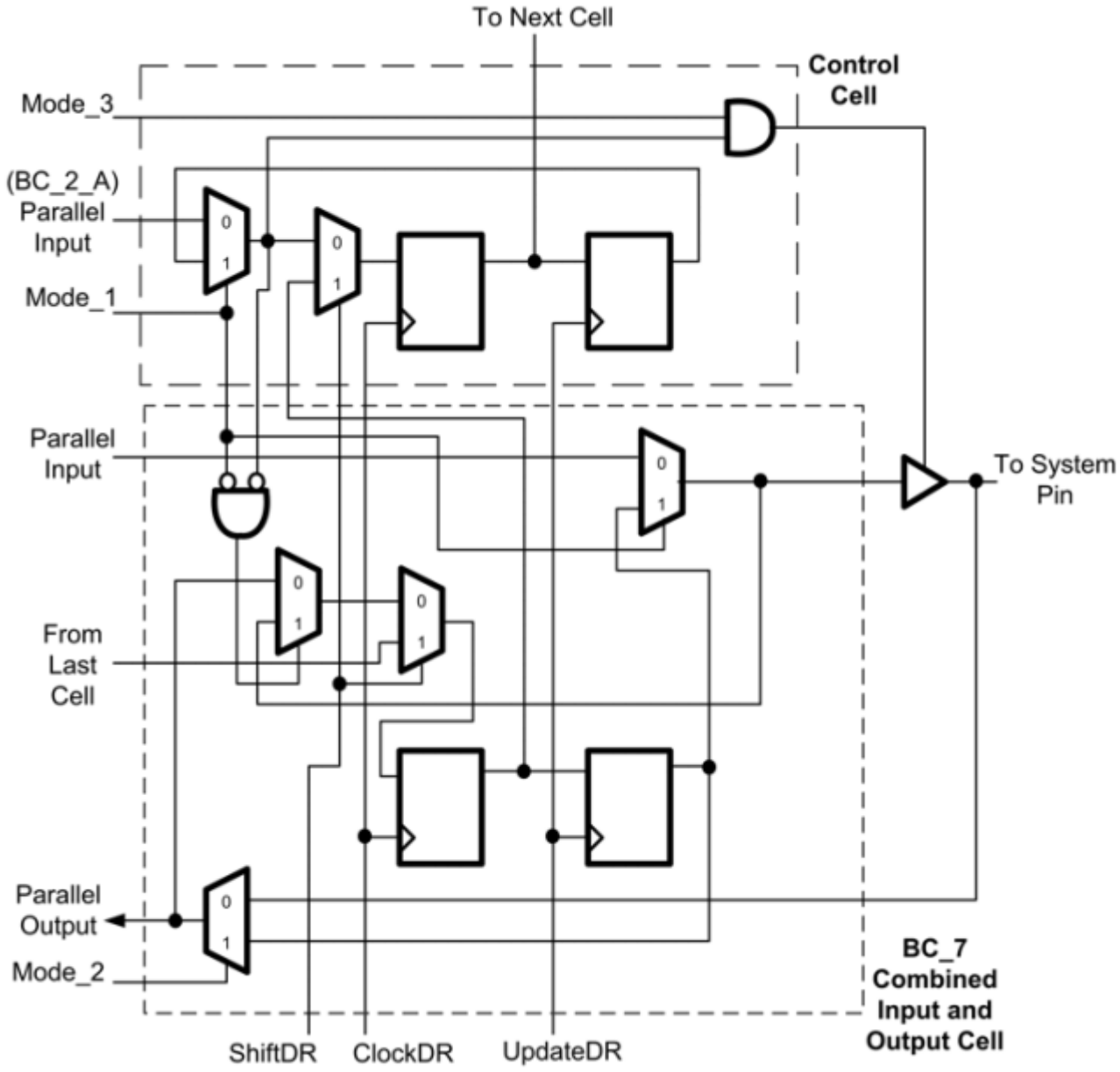
8.9 BC_7

Figure A-9. BC_7 Type Cell Shown with BC_2_A Control Cell



8.10 BC_7_LOW

Figure A-10. BC_7_LOW Type Cell Shown with BC_2_A Control Cell



8.11 BC_8

Figure A-11. BC_8 Type Cell with an Open-Collector L-Type Pad

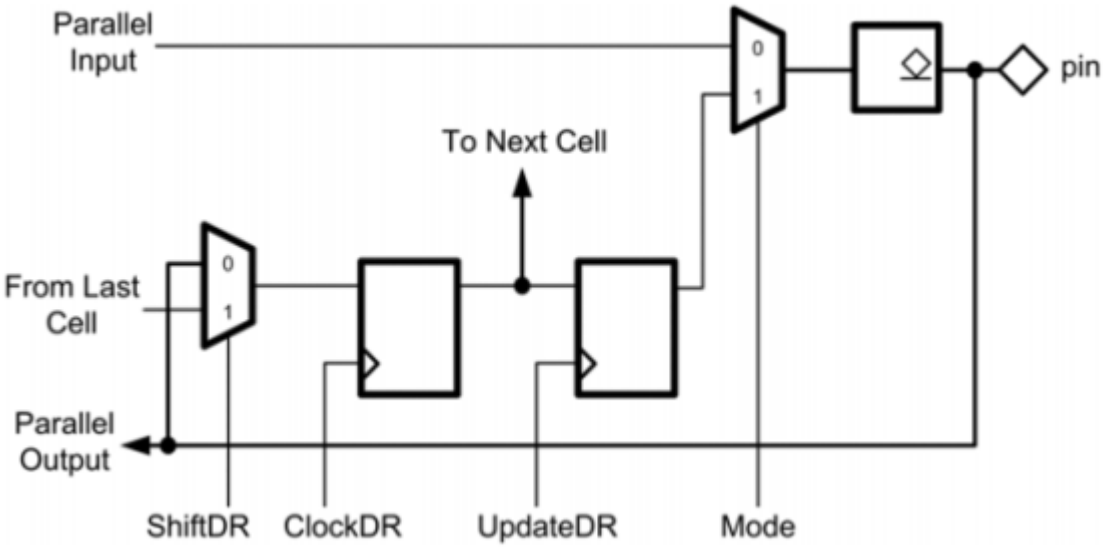
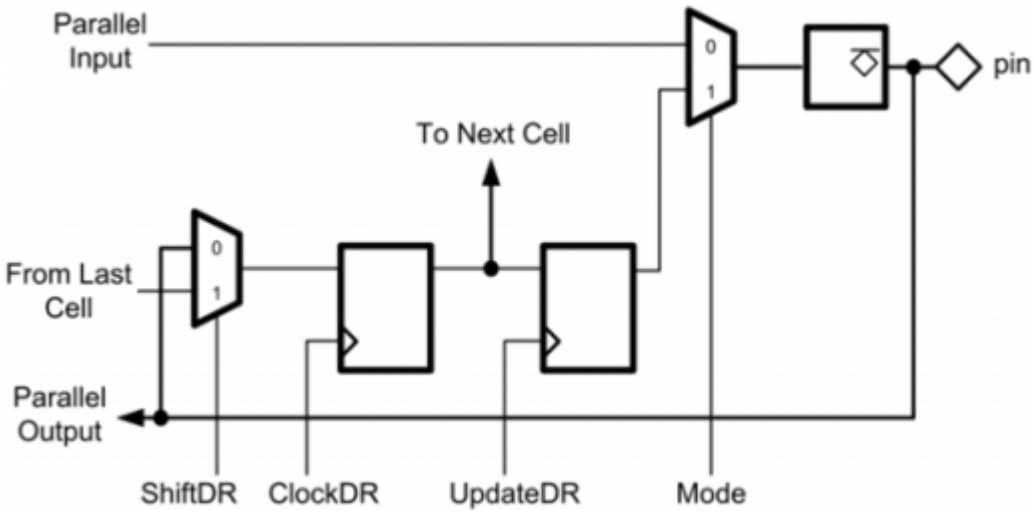
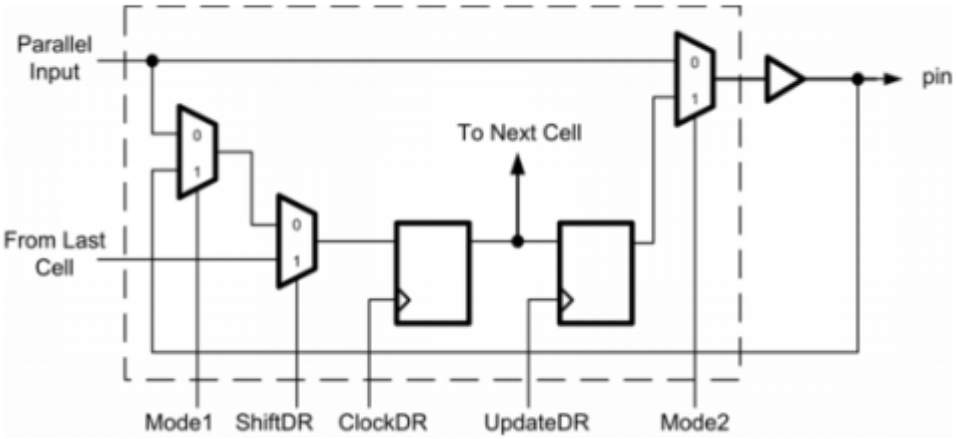


Figure A-12. BC_8 Type Cell with an Open-Collector H-Type Pad



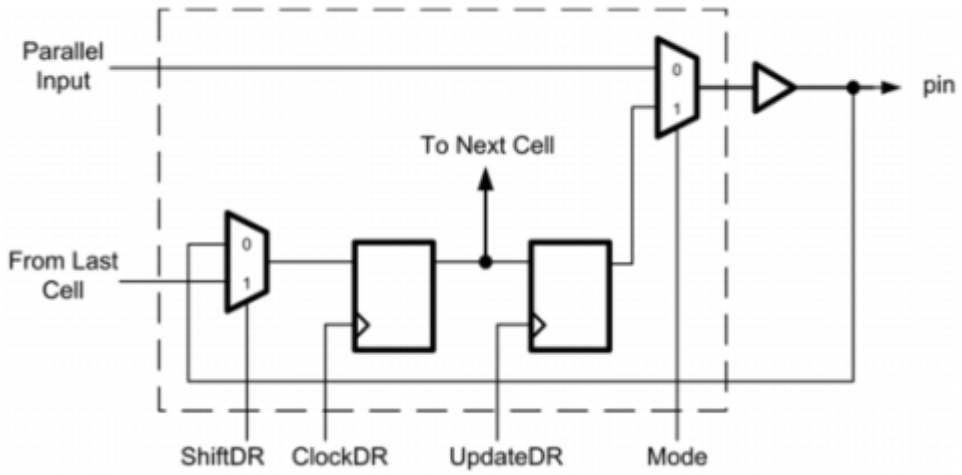
8.12 BC_9

Figure A-13. BC_9 Type Cell



8.13 BC_10

Figure A-14. BC_10 Type Cell

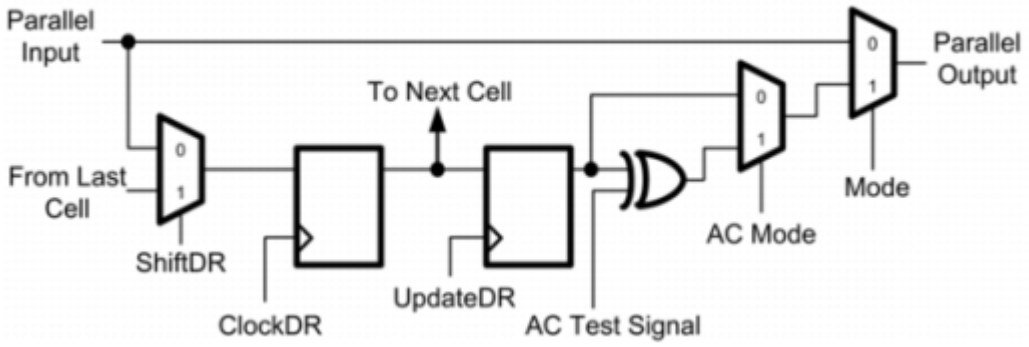


9. tessent AC cell

ref: bsda_ref.pdf

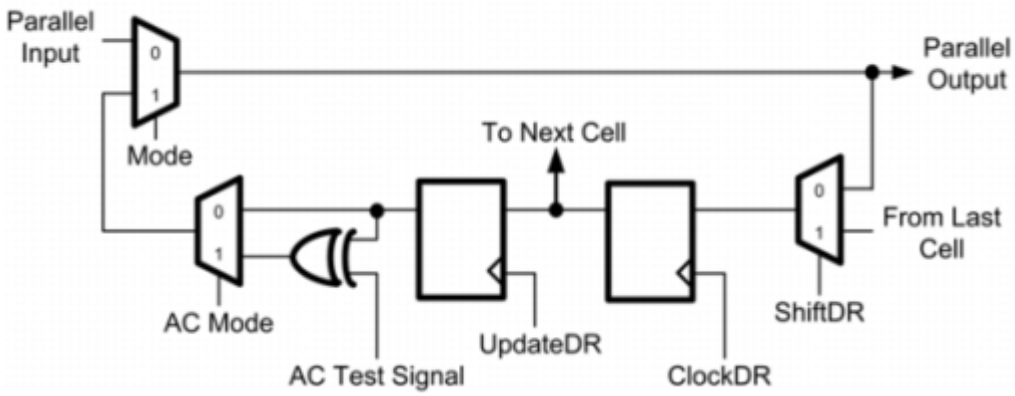
9.1 AC_1

Figure A-15. AC_1 Type Cell



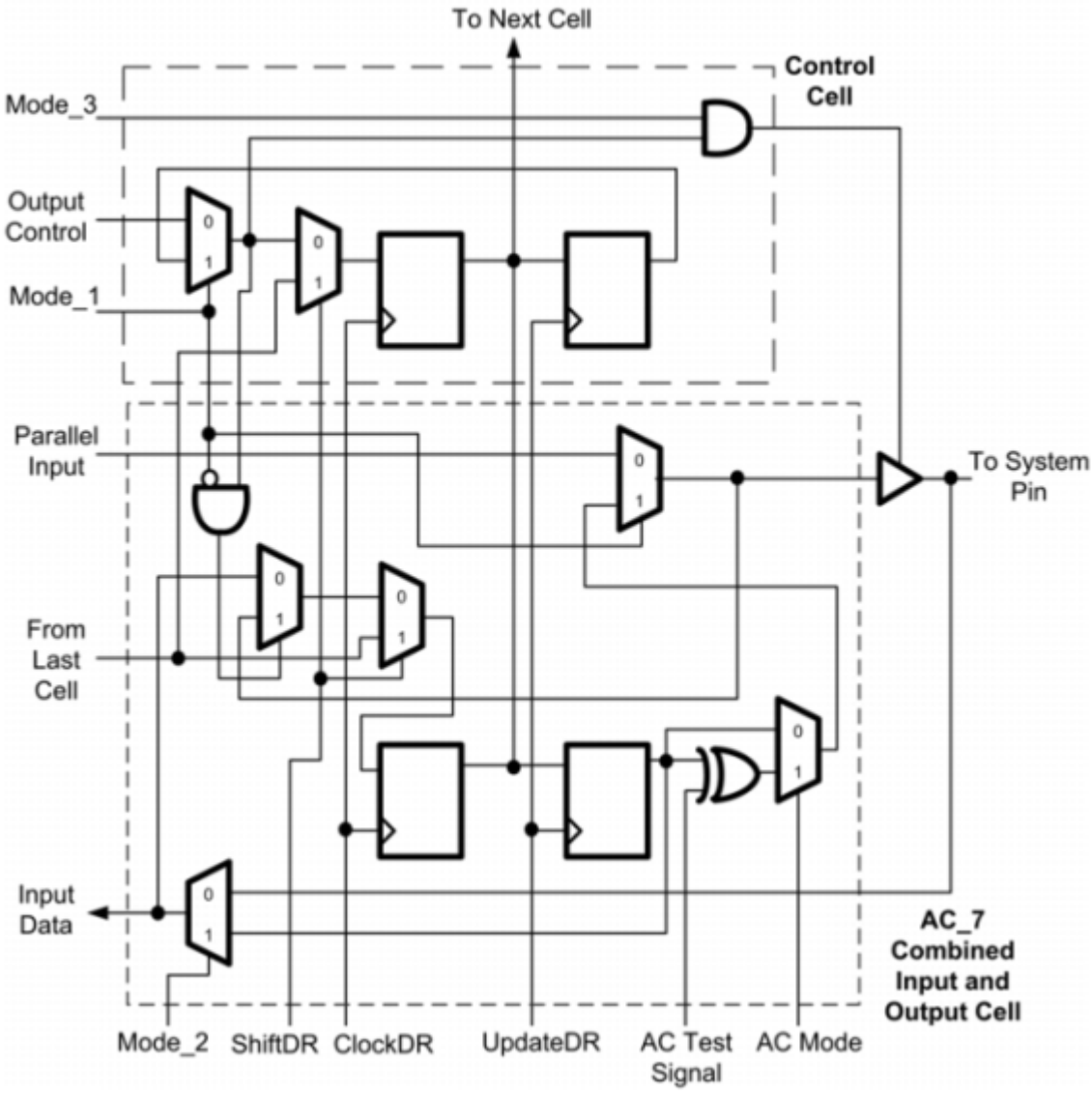
9.2 AC_2

Figure A-16. AC_2 Type Cell



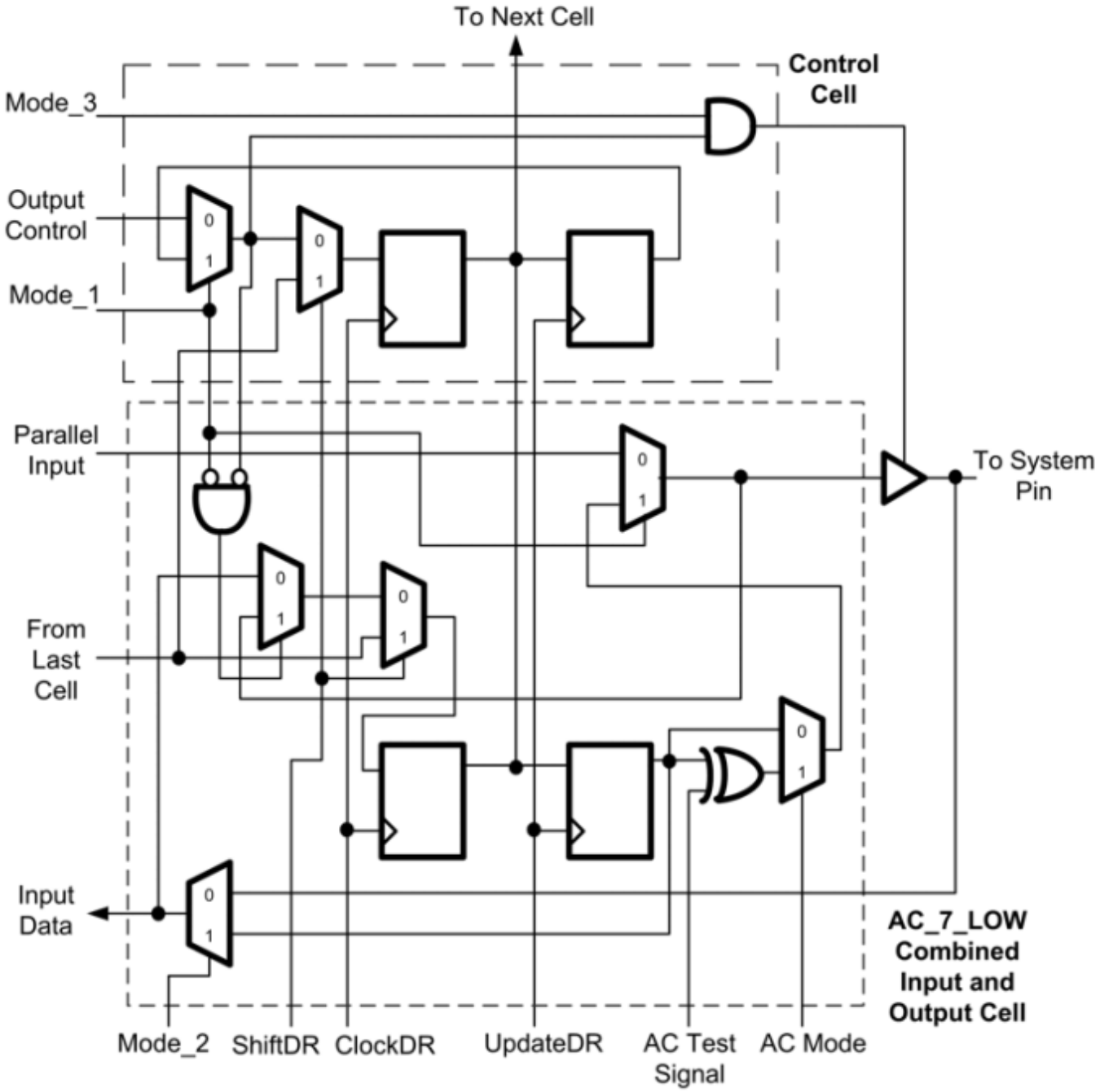
9.3 AC_7

Figure A-17. AC_7 Type Cell



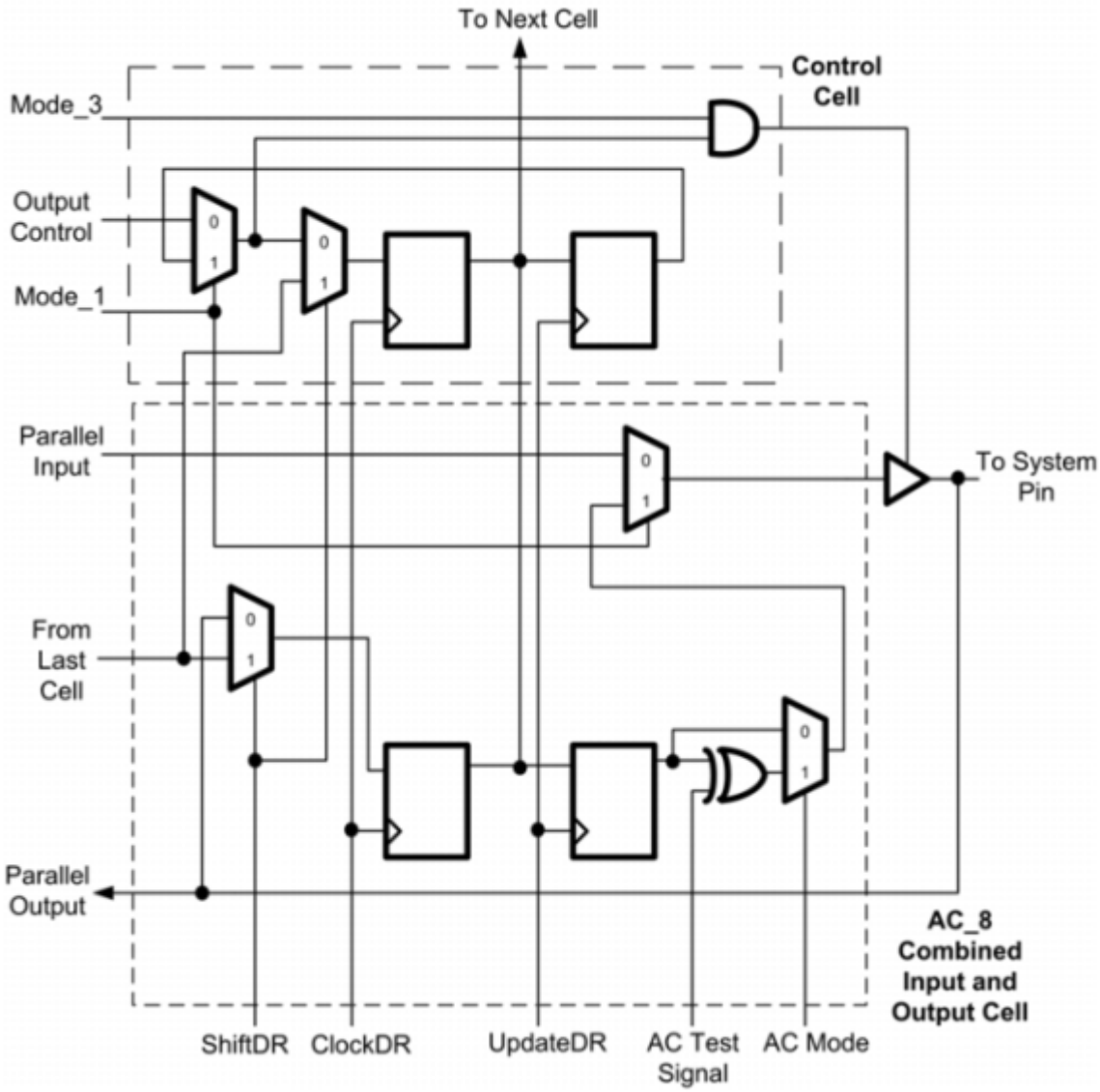
9.4 AC_7_LOW

Figure A-18. AC_7_LOW Type Cell Shown with BC_2_A Control Cell



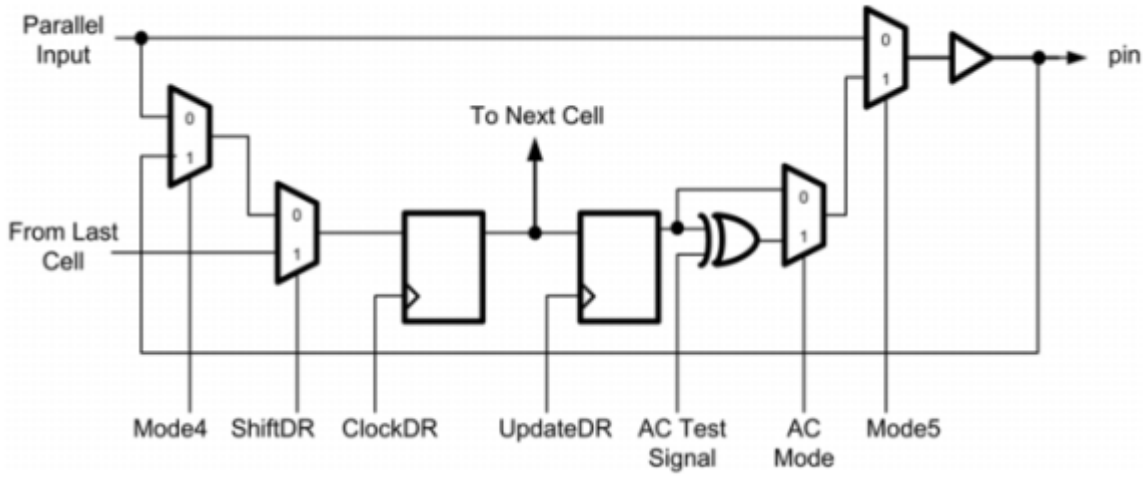
9.5 AC_8

Figure A-19. AC_8 Type Cell



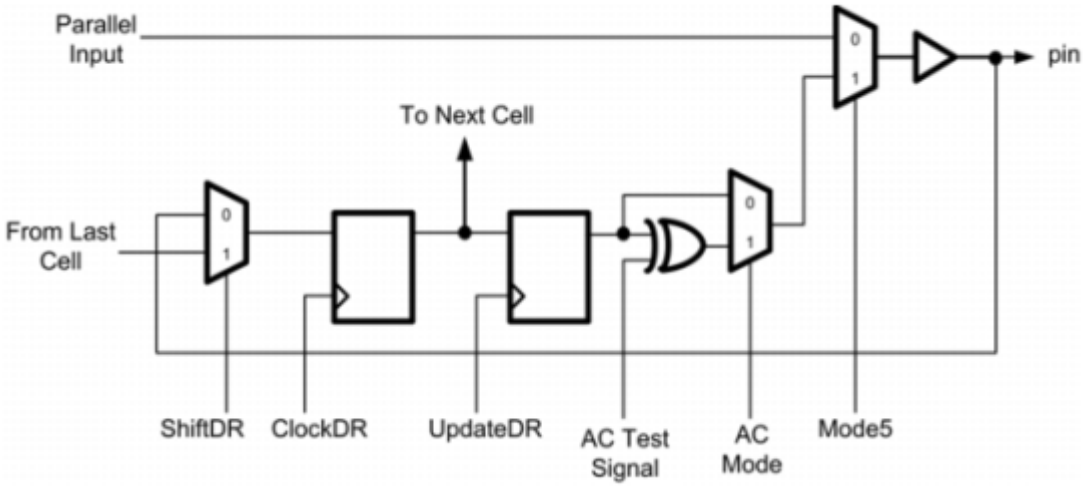
9.6 AC_9

Figure A-20. AC_9 Type Cell



9.7 AC_10

Figure A-21. AC_10 Type Cell



10. IEEE 1149.1 BSCAN BC cell

- BC_1, input cell, control cell, capture misson input
- BC_2, input cell, control cell, capture misson output
- BC_4, Observe-only input cell without control
- BC_7, BIDI双向 data cell; capture UPD/PAD input/misson output
- BC_8, BIDI双向 data cell; capture PAD output
- BC_9, self-monitor output cell; mode 4 capture PAD output, else capture mission input
- BC_10, self-monitor output cell; capture PAD output only

10.1 BC_1

mode

Table 11-3—Mode signal generation for the example cell in Figure 11-19

Precedence	Instruction (Condition)	Mode1
1	(Cell in excluded segment)	0
2	*EXTEST*	1
	INTEST	1
3	(TMP controller *Persistence_on* state)	1
4	*PRELOAD*	0
	SAMPLE	0
	RUNBIST	1
	CLAMP	1
	CLAMP_HOLD	1
	CLAMP_RELEASE	1
	INIT_SETUP_CLAMP	1
	INIT_RUN	1
	Nonboundary instruction	0

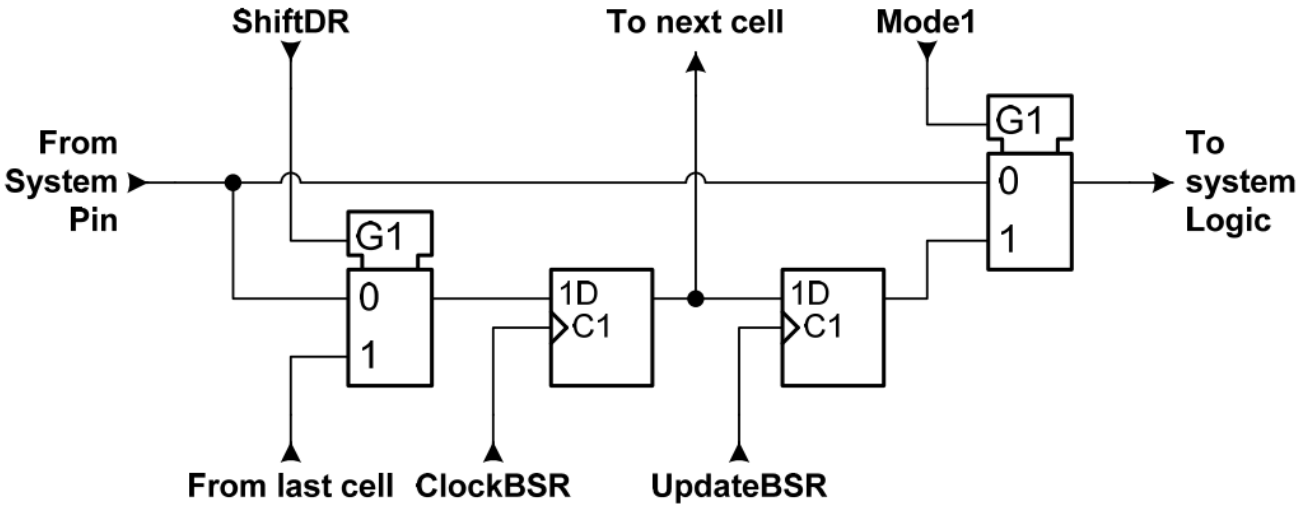


Figure 11-19—Input cell that supports all instructions [BC_1]

10.2 BC_2

Table 11-2—Mode signal generation for the example cells in Figure 11-15 and Figure 11-16

Precedence	Instruction (Condition)	Mode2
1	(Cell in excluded segment)	0
2	*EXTEST*	0
	INTEST	1
3	(TMP controller *Persistence_on* state)	1
4	*PRELOAD*	0
	SAMPLE	0
	RUNBIST	X
	CLAMP	X
	CLAMP_HOLD	1
	CLAMP_RELEASE	1
	INIT_SETUP_CLAMP	1
	INIT_RUN	1
	Nonboundary instruction	0

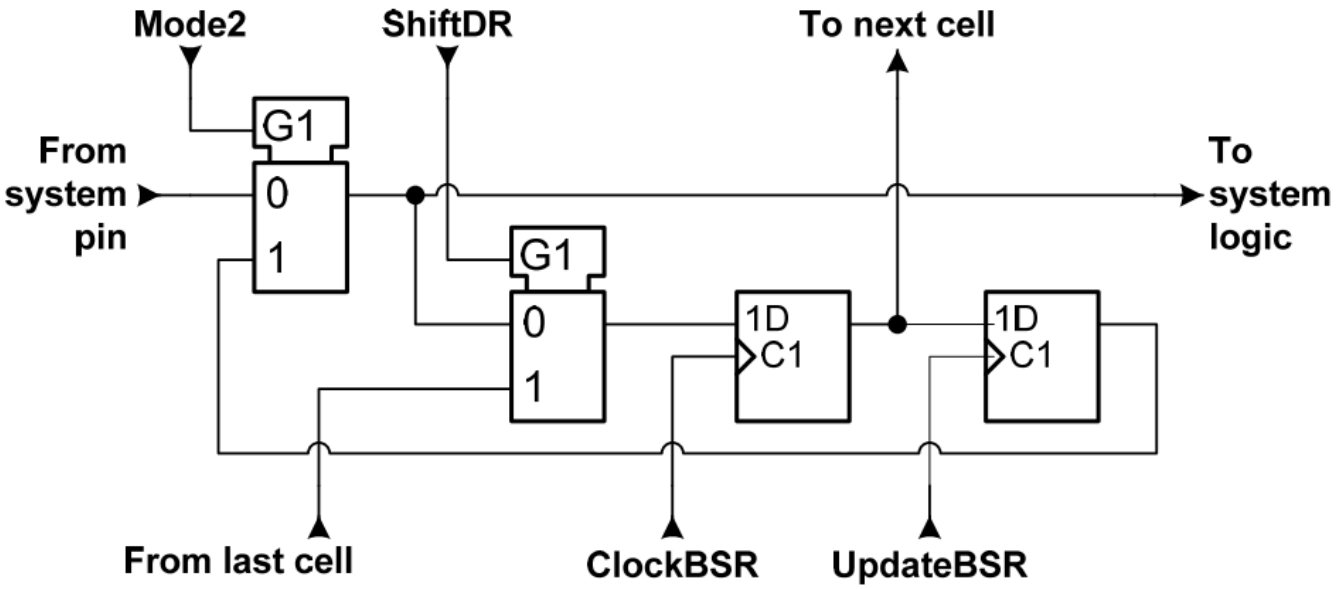


Figure 11-15—Input cell with parallel output register [BC_2]

10.3 BC_3

个人觉得BC_3不会使用

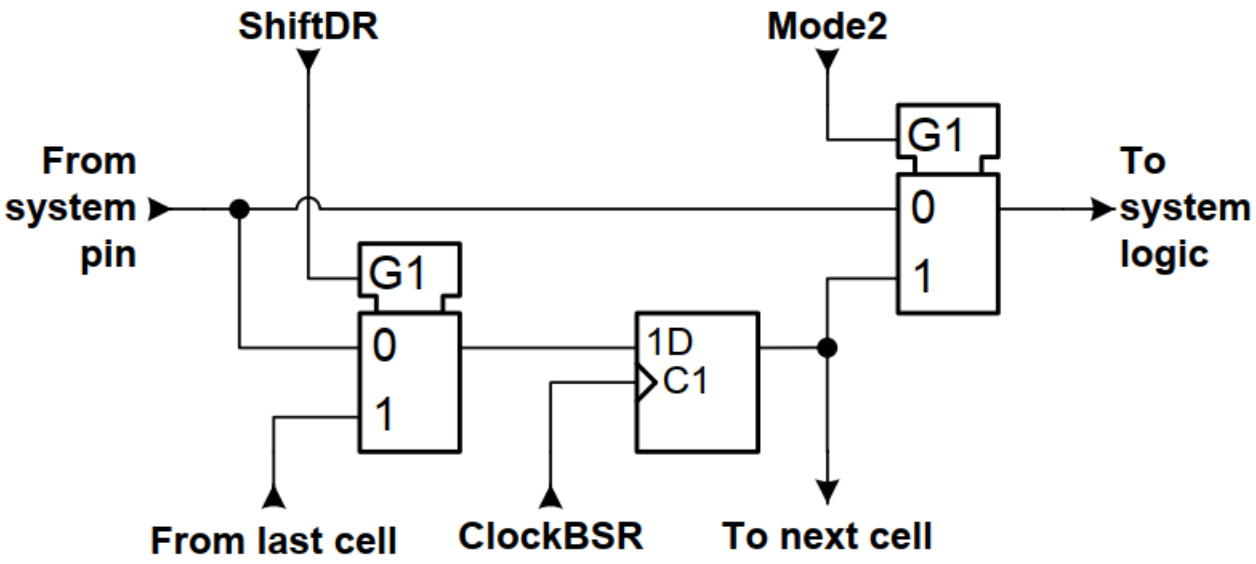


Figure 11-16—Input cell without parallel output register [BC_3]

10.4 BC_4

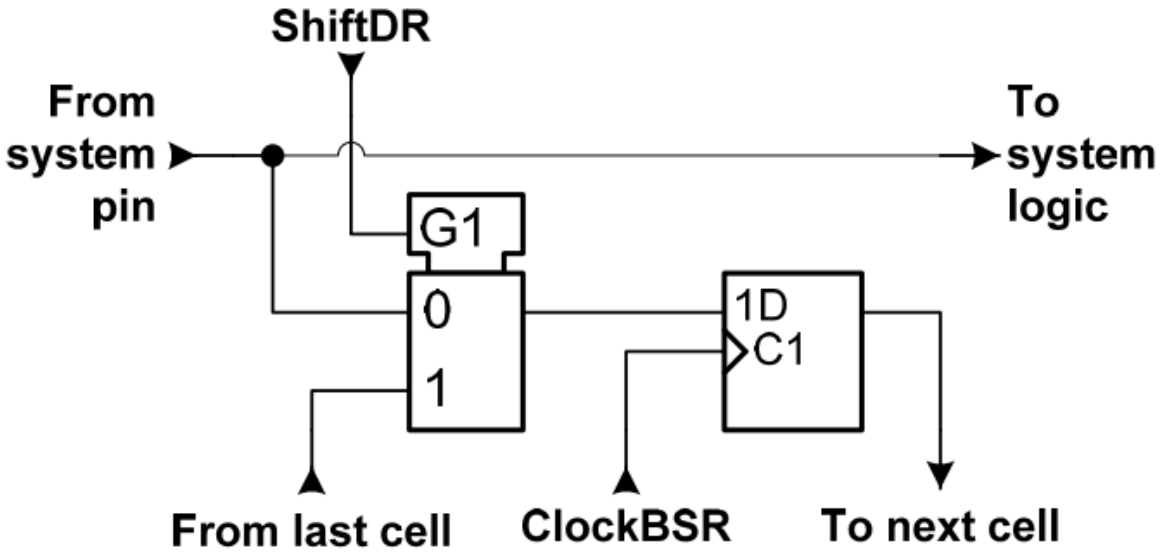


Figure 11-18—Observe-only input cell without control [BC_4]

10.5 BC_5

Table 11-6—Mode signal generation for the example cells in Figure 11-31, Figure 11-35, Figure 11-37, and Figure 11-47

Precedence	Instruction (Condition)	Mode1
1	(Cell in excluded segment)	0
2	*EXTEST*	1
	INTEST	1
3	(TMP controller *Persistence_on* state)	1
4	*PRELOAD*	0
	SAMPLE	0
	RUNBIST	1
	CLAMP	1
	CLAMP_HOLD	1
	CLAMP_RELEASE	1
	INIT_SETUP_CLAMP	1
	INIT_RUN	1
	Nonboundary instruction	0

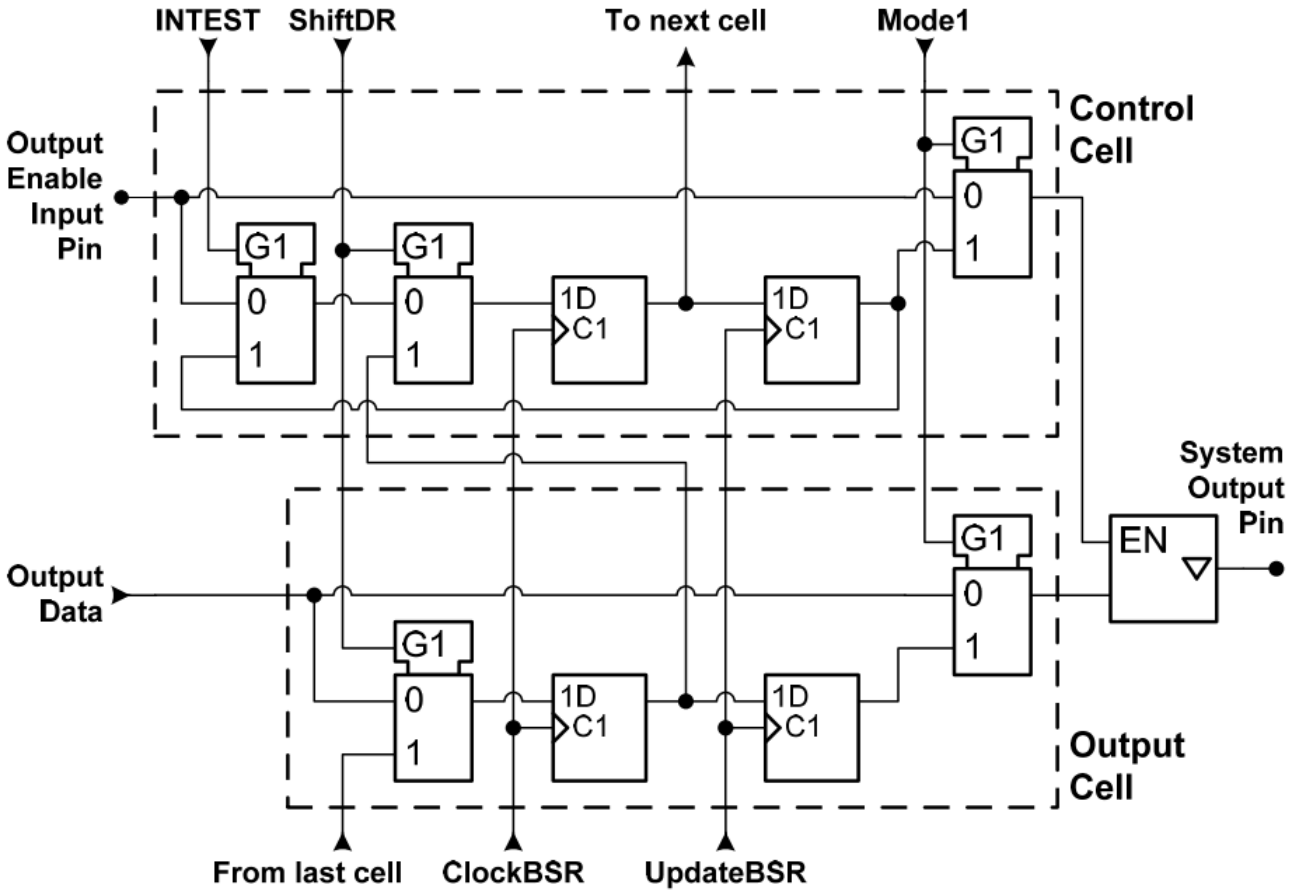


Figure 11-47—Boundary-scan register cells at a three-state pin where output control is from a system pin [BC_5, control; BC_1, data]

10.6 BC_7

Table 11-10—Mode signal generation for the example cells in Figure 11-38

Precedence	Instruction (Condition)	Mode5	Mode2	Mode6
1	(Cell in excluded segment)	0	0	1
2	*EXTEST*	1	0	1
	INTEST	0	1	0
3	(TMP controller *Persistence_on* state)	1	1	1
4	*PRELOAD*	0	0	1
	SAMPLE	0	0	1
	RUNBIST	0	X	0
	CLAMP	1	X	1
	CLAMP_HOLD	1	1	1
	CLAMP_RELEASE	1	1	1
	INIT_SETUP_CLAMP	1	1	1
	INIT_RUN	1	1	1
	HIGHZ	X	X	0
	Nonboundary instruction	0	0	1

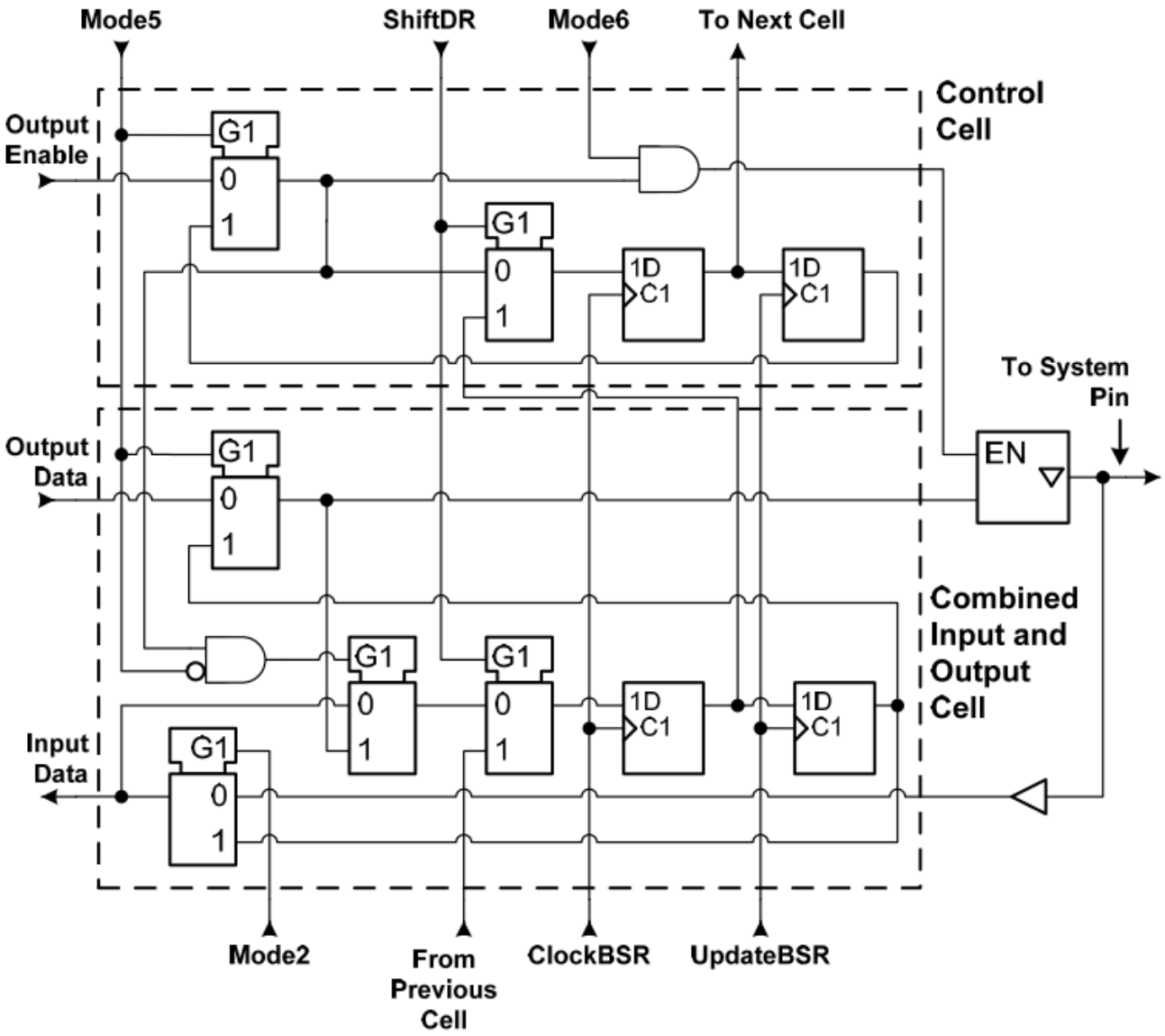


Figure 11-38—Boundary-scan register cells at a bidirectional pin—Example 2 [BC_2 control; BC_7 data]

10.7 BC_8

mode

Table 11-12—Mode signal generation for the example cells in Figure 11-41 and Figure 11-42

Precedence	Instruction (Condition)	Mode7
1	(Cell in excluded segment)	0
2	*EXTEST*	1
3	(TMP controller *Persistence_on* state)	1
4	*PRELOAD*	0
	SAMPLE	0
	RUNBIST	X
	CLAMP	1
	CLAMP_HOLD	1
	CLAMP_RELEASE	1
	INIT_SETUP_CLAMP	1
	INIT_RUN	1
	Nonboundary instruction	0

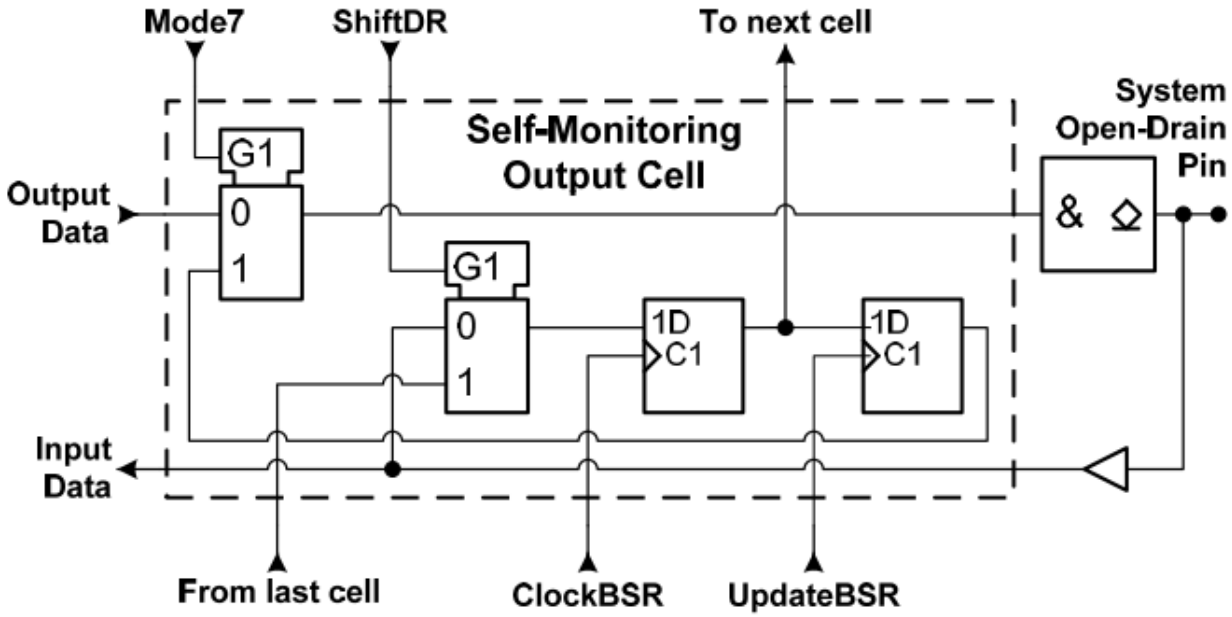


Figure 11-41—Boundary-scan register cell at an open-collector bidirectional pin [BC_8]

bc_2 control + bc_8

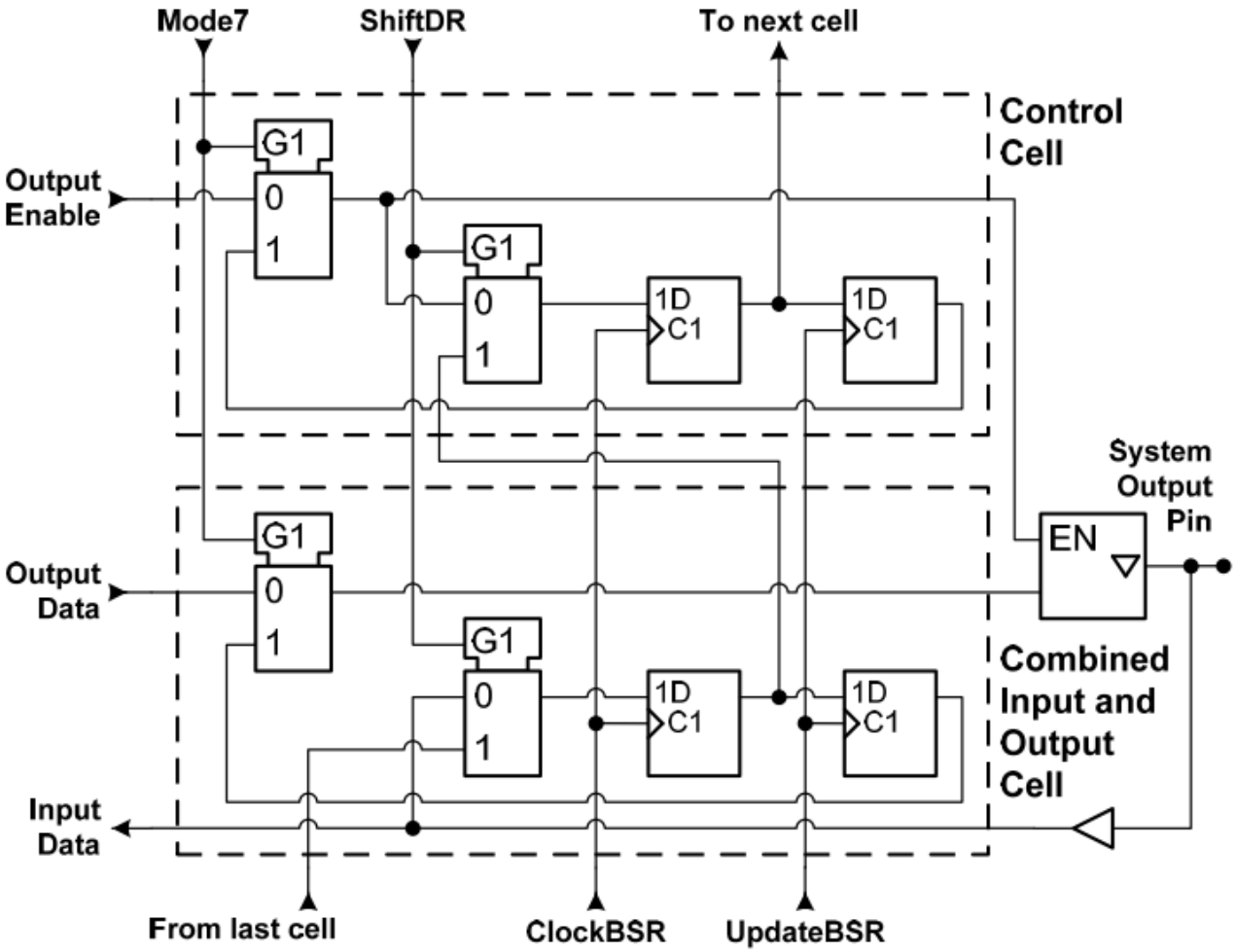


Figure 11-42—Boundary-scan register cells for use at a bidirectional pin where *INTEST* is not provided [BC_2, control; BC_8, data]

10.8 BC_9

Table 11-8—Mode signal generation for the example cell in Figure 11-33

Precedence	Instruction (Condition)	Mode4	Mode1
1	(Cell in excluded segment)	0	0
2	*EXTEST*	1	1
	INTEST	0	1
3	(TMP controller *Persistence_on* state)	X	1
4	*PRELOAD*	X	0
	SAMPLE	0	0
	RUNBIST	X	1
	CLAMP	X	1
	CLAMP_HOLD	X	1
	CLAMP_RELEASE INIT_SETUP_CLAMP	X	1
	INIT_RUN	X	1
	Nonboundary instruction	0	0

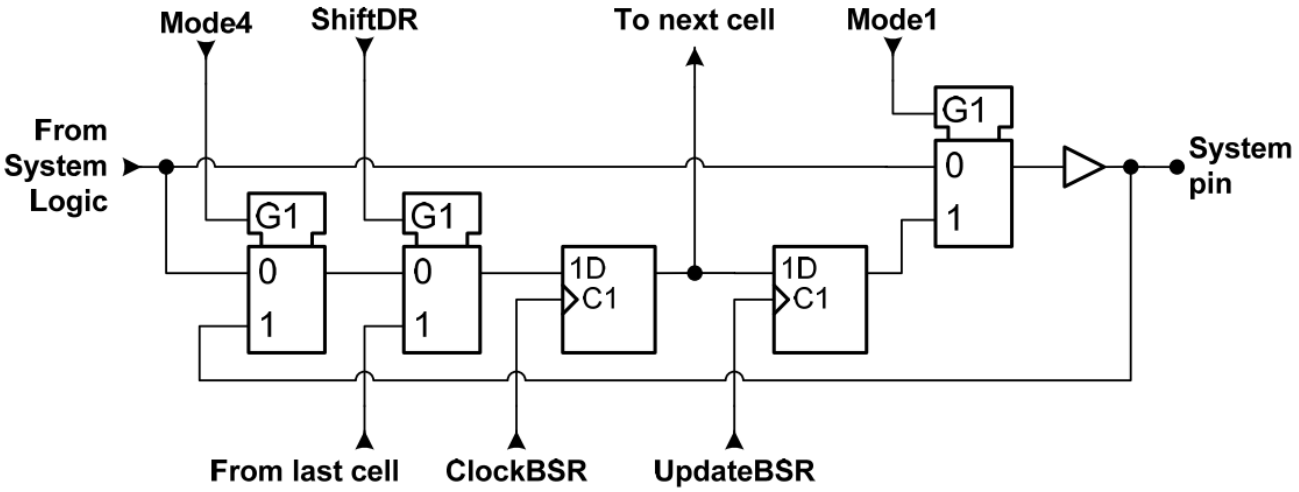


Figure 11-33—Self-monitoring output cell that supports *INTEST* [BC_9]

10.9 BC_10

Table 11-7—Mode signal generation for the example cells in Figure 11-32, Figure 11-34, and Figure 11-40

Precedence	Instruction (Condition)	Mode3
1	(Cell in excluded segment)	0
2	*EXTEST*	1
3	(TMP controller *Persistence_on* state)	1
4	*PRELOAD*	0
	SAMPLE	0
	RUNBIST	1
	CLAMP	1
	CLAMP_HOLD	1
	CLAMP_RELEASE INIT_SETUP_CLAMP	1
	INIT_RUN	1
	Nonboundary instruction	0
NOTE—Mode3 is the same as Mode1 except that the *INTEST* instruction is not supported.		

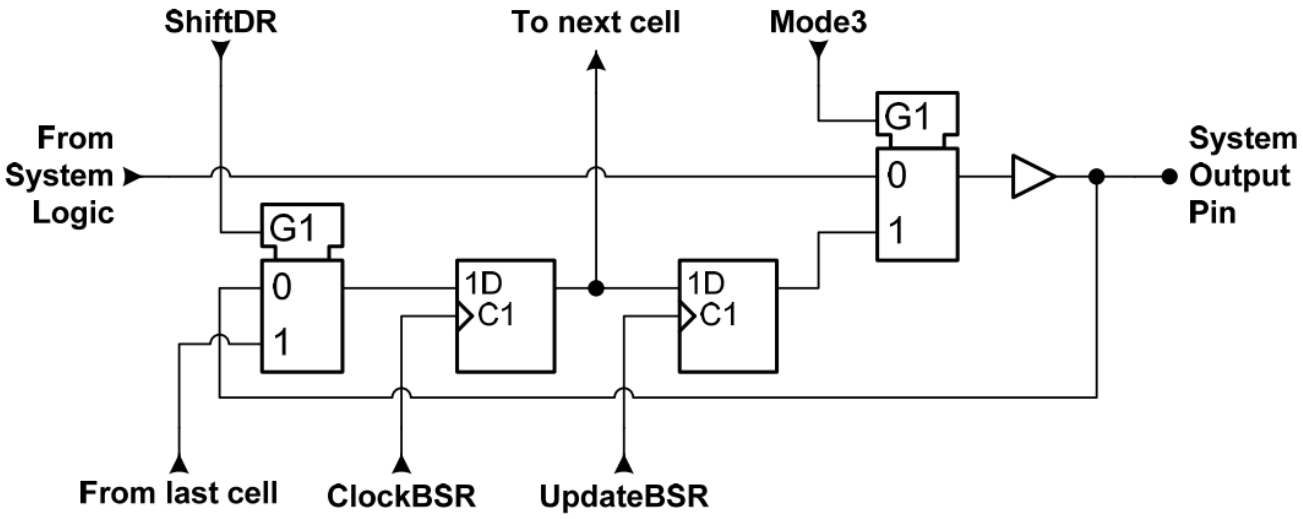


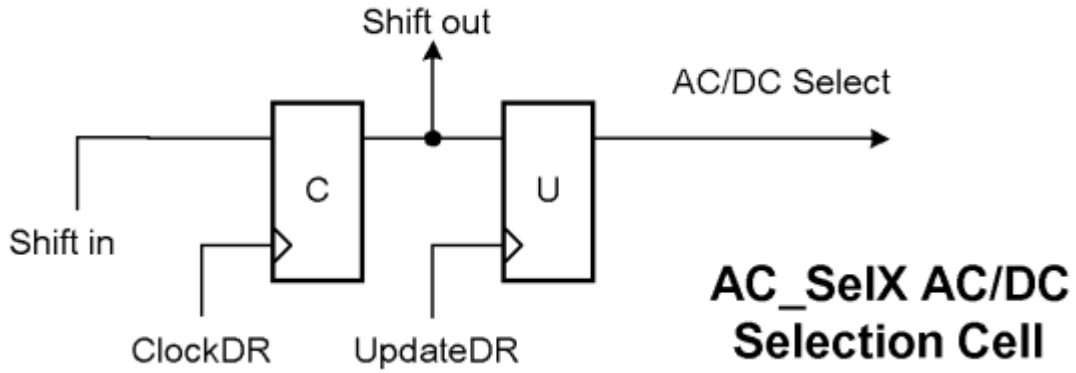
Figure 11-34—Self-monitoring output cell that does not support *INTEST* [BC_10]

11. BSCAN AC cell

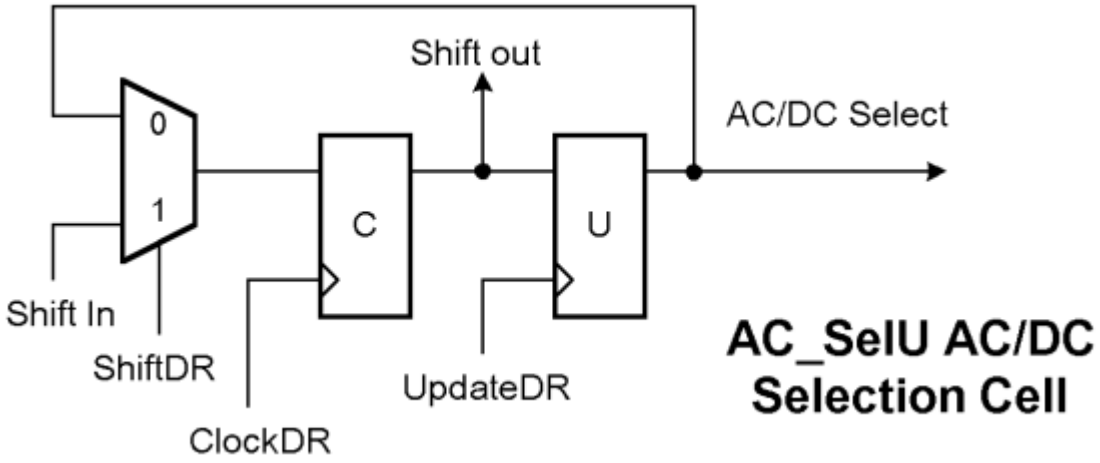
- AC_SelX, 控制选择AC/DC测试模式， capture的值永远是X，即不关注capture到的值
- AC_SelU, 控制选择AC/DC测试模式， capture的值是UPD，即capture到的值是上一次配置的AC/DC的选择值。
- AC_1, input cell, control cell, capture misson input
- AC_2, input cell, control cell, capture misson output
- AC_7, BIDI双向 data cell; capture UPD/PAD input/misson output
- AC_8, BIDI双向 data cell; capture PAD output
- AC_9, self-monitor output cell; mode 4 capture PAD output, else capture mission input
- AC_10, self-monitor output cell; capture PAD output only

	mode 1	**mode 2**	**mode 3**	**mode 4**	**mode 5**
EXTEST	1	0	1	1	1
PRELOAD	0	0	1	X	0
SAMPLE	0	0	1	0	0
INTEST	0	1	0	0	1
RUNBIST	X	X	0	X	1
CLAMP	1	X	1	X	1
HIGHZ	X	X	0	X	X
NOTES: 1. EXTEST inluce EXTEST, EXTEST_PLUSE, EXTEST_TRAIN					

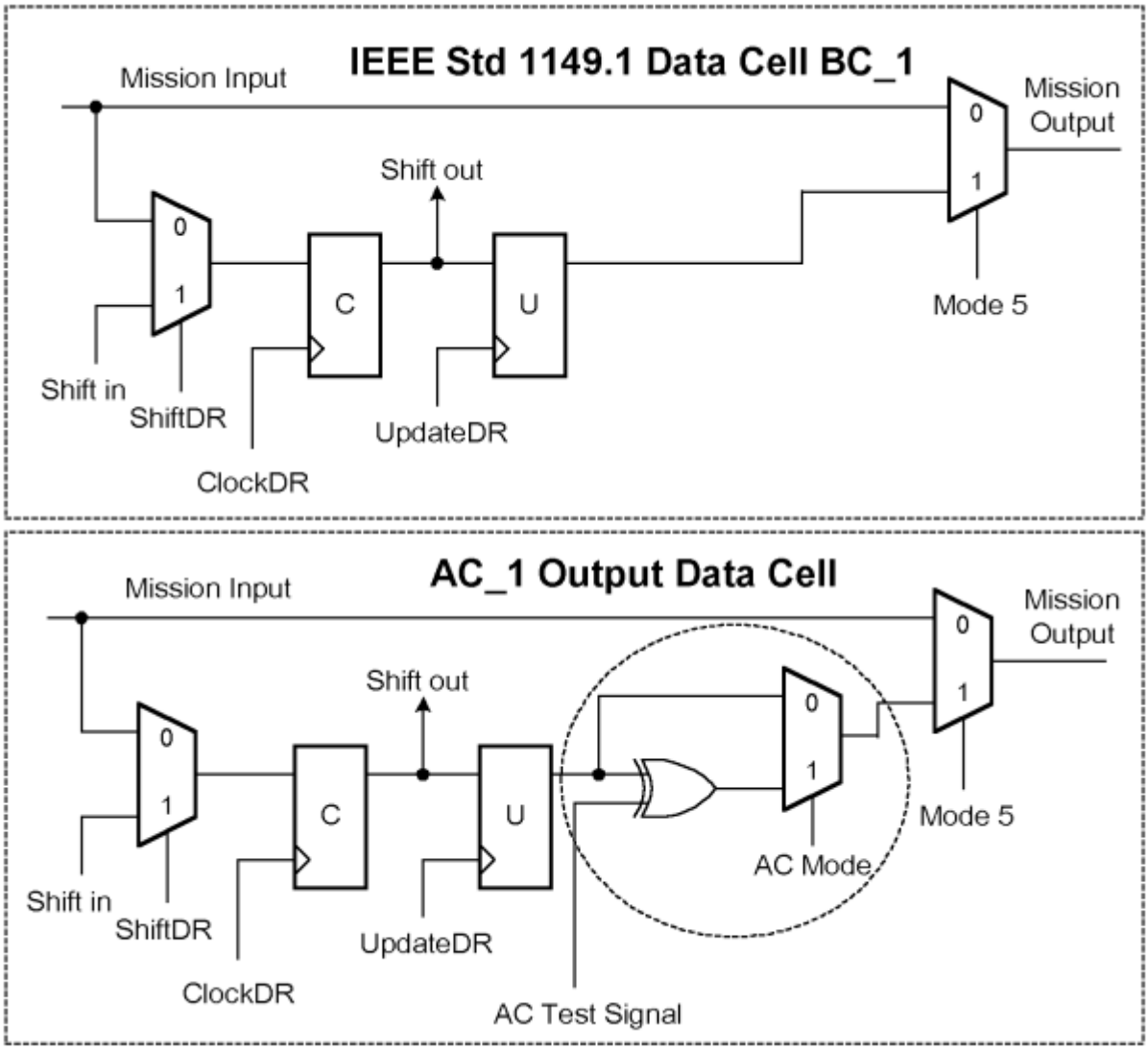
11.1 AC_SelX



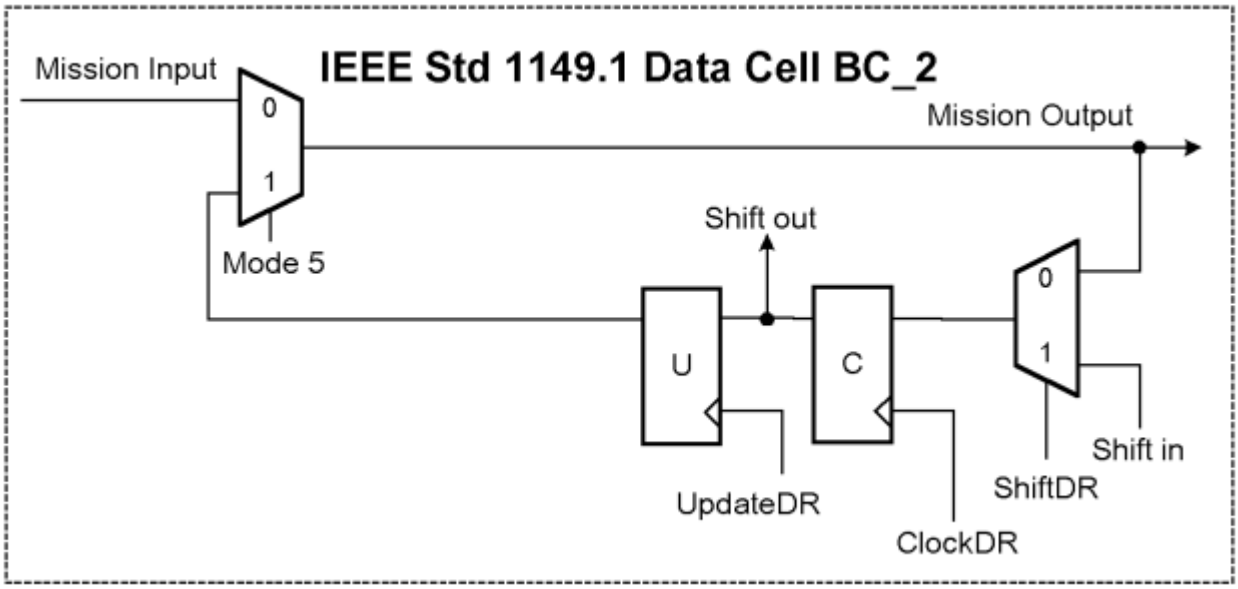
11.2 AC_SelU

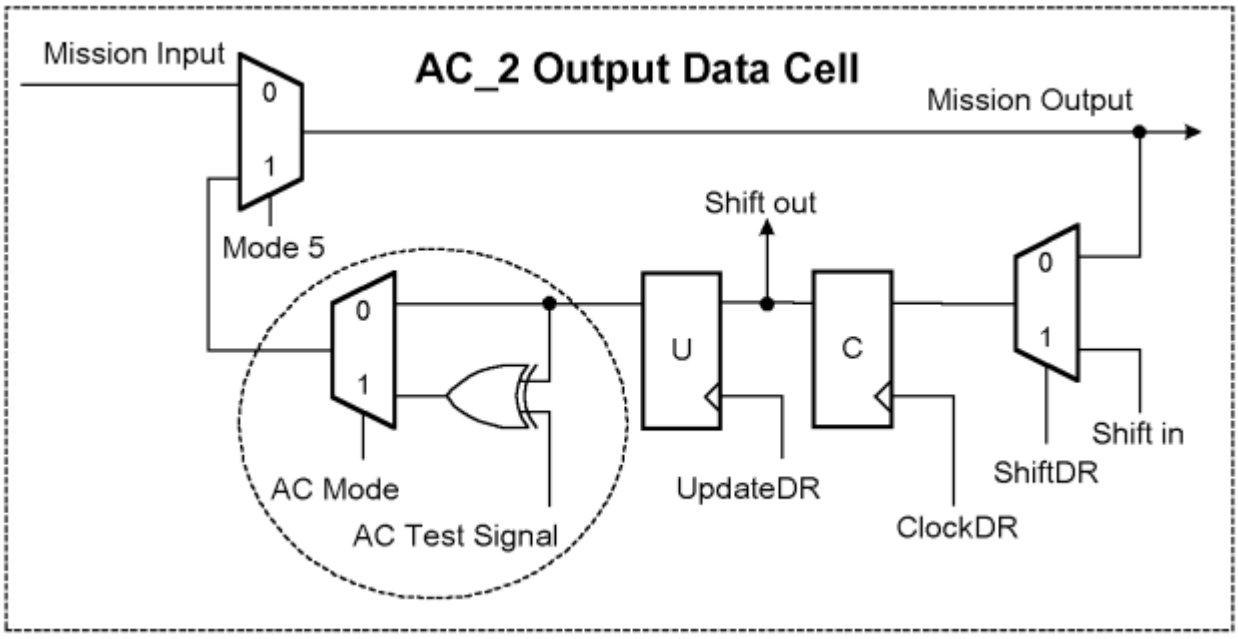


11.3 AC_1

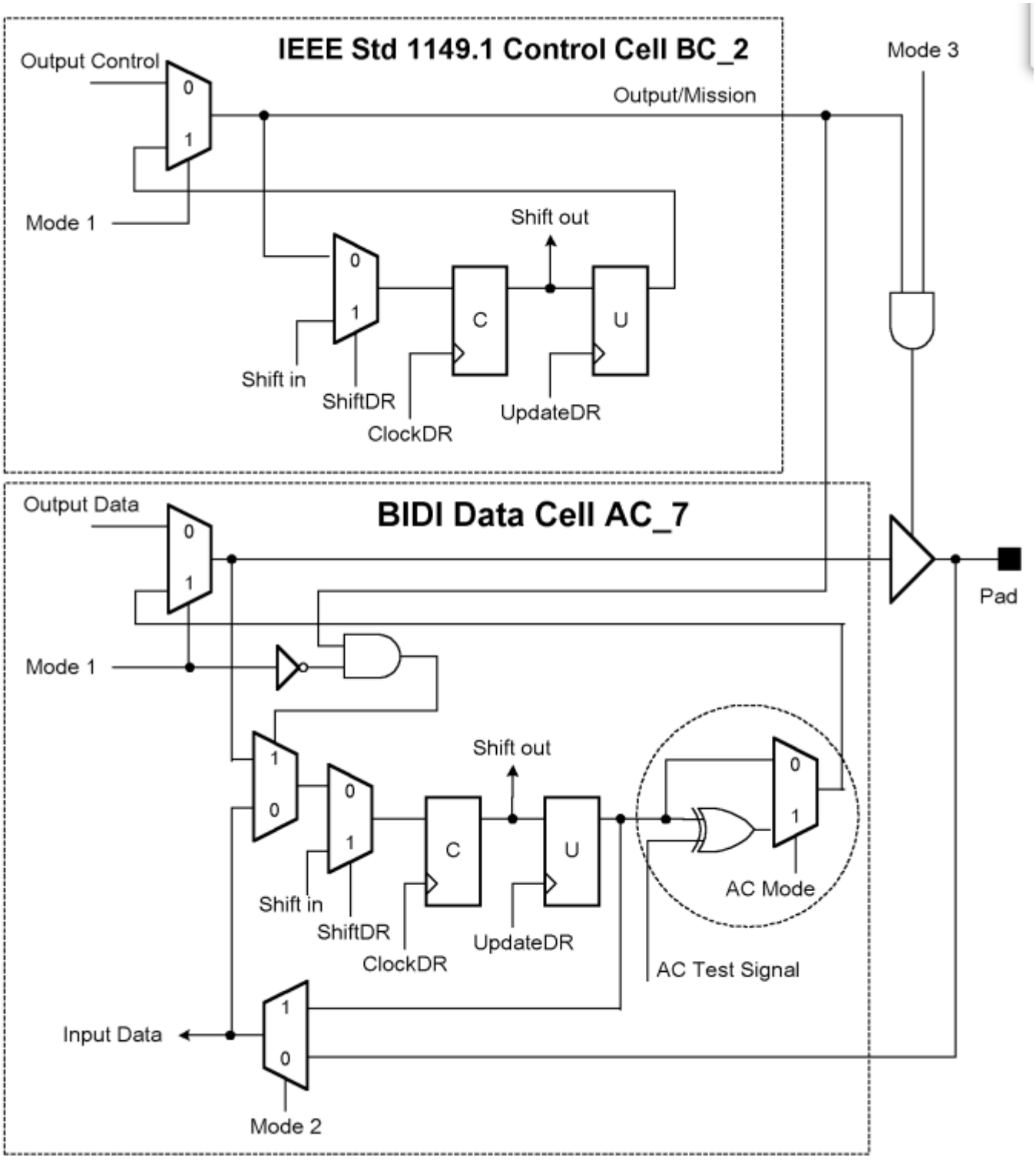

IEEE Std 1149.1 Data Cell BC_1
Mission Input
Mission Output
Shift out
0
1
C
U
Mode 5
Shift in
ShiftDR
ClockDR
UpdateDR
AC_1 Output Data Cell
Mission Input
Mission Output
Shift out
0
1
C
U
Mode 5
AC Mode
Shift in
ShiftDR
ClockDR
UpdateDR
AC Test Signal

11.4 AC_2

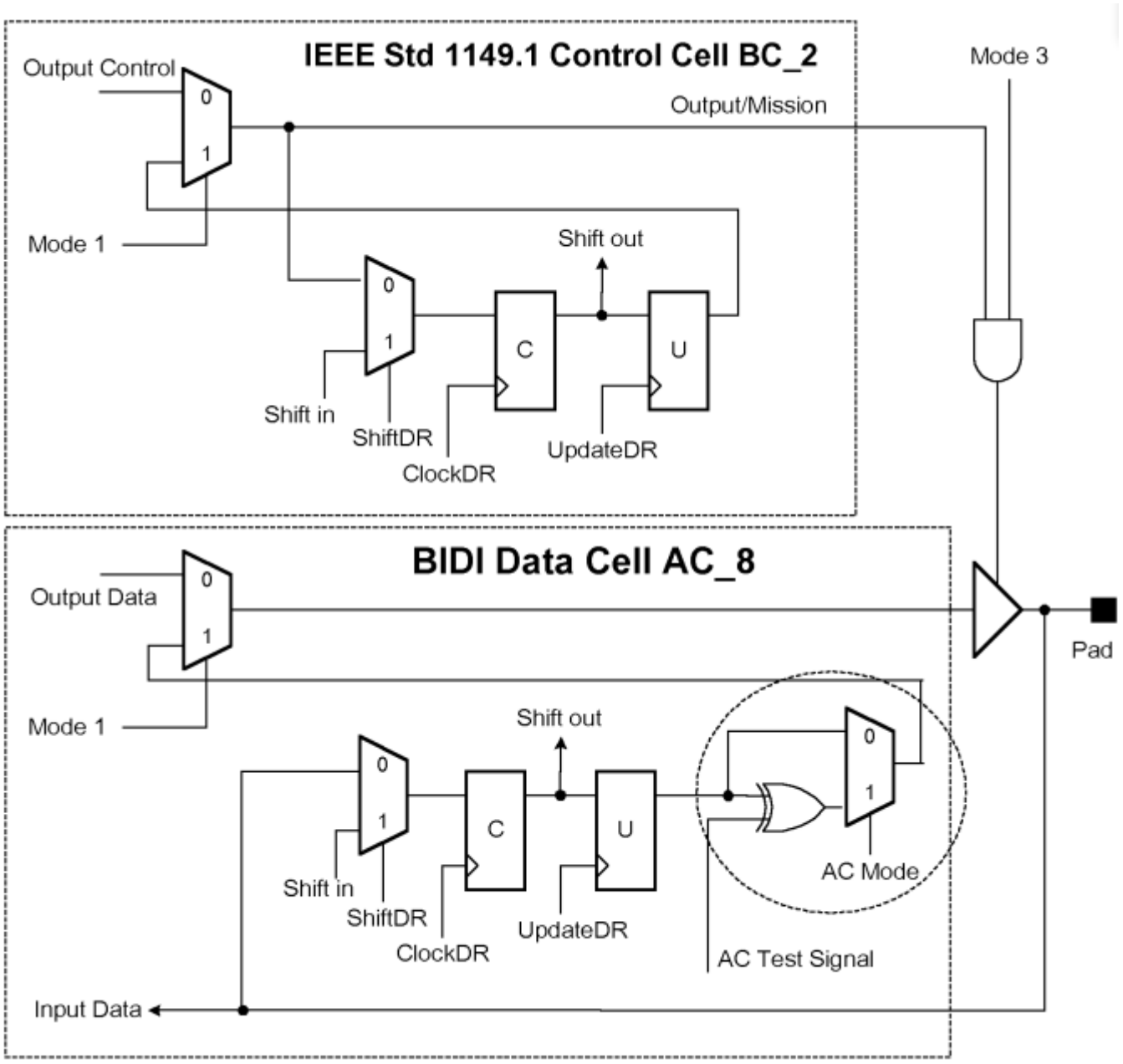

IEEE Std 1149.1 Data Cell BC_2
Mission Input
Mission Output
Mode 5
Shift out
U
C
Shift in
UpdateDR
ShiftDR
ClockDR


AC_2 Output Data Cell
Mission Input
Mission Output
Mode 5
Shift out
AC Mode
AC Test Signal
U
C
Shift in
UpdateDR
ShiftDR
ClockDR

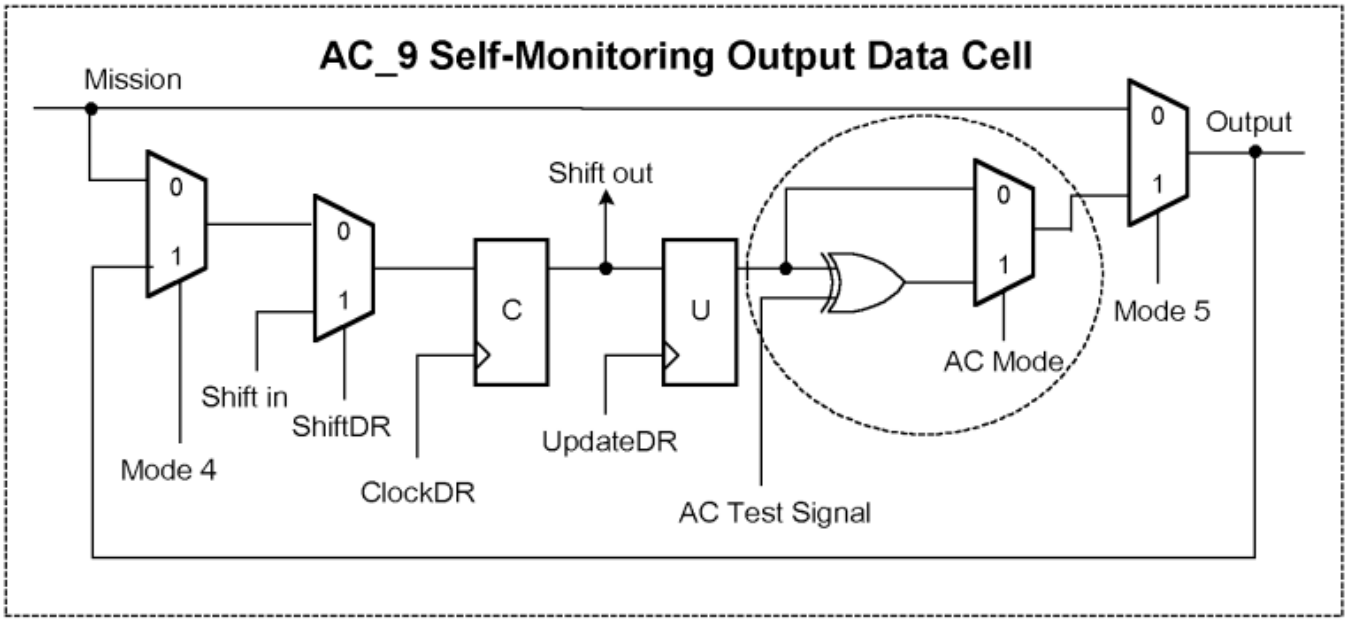
11.5 AC_7


IEEE Std 1149.1 Control Cell BC_2
Output Control
Output/Mission
Mode 3
Mode 1
Shift out
Shift in
ShiftDR
ClockDR
UpdateDR
C
U
BIDI Data Cell AC_7
Output Data
Pad
Mode 1
Shift out
Shift in
ShiftDR
ClockDR
UpdateDR
AC Mode
AC Test Signal
Input Data
Mode 2

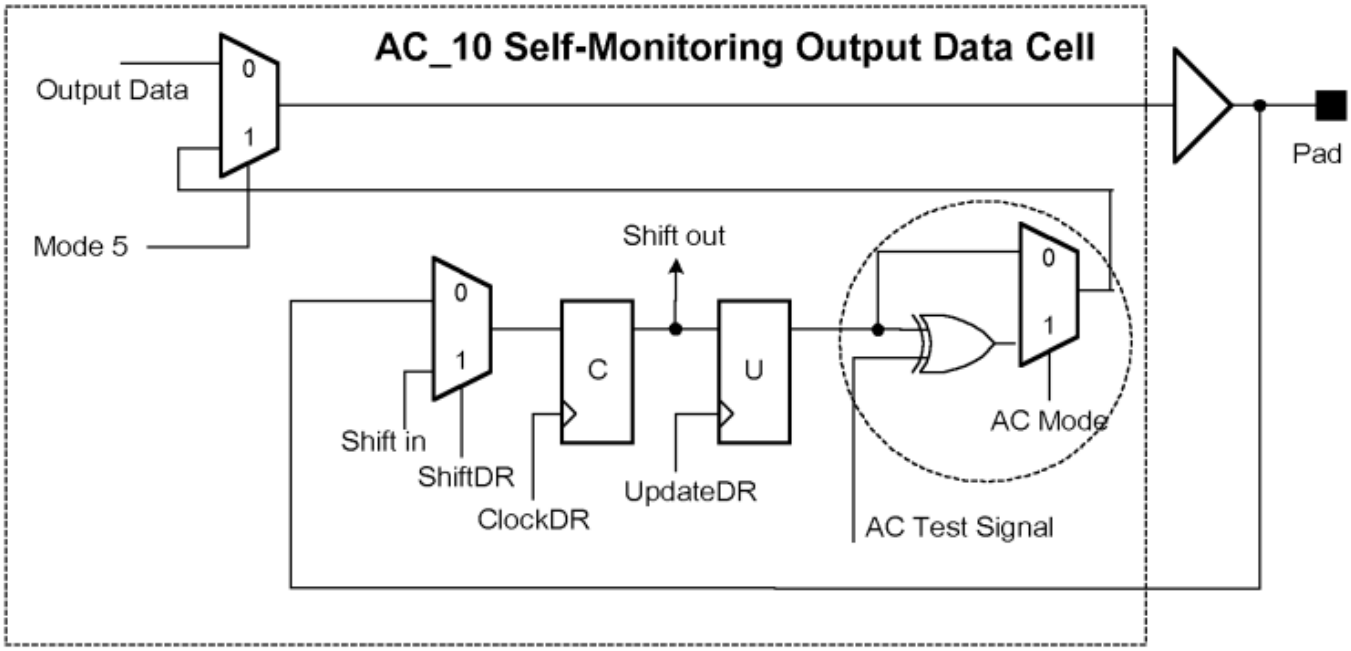
11.6 AC_8


IEEE Std 1149.1 Control Cell BC_2
Output Control
Output/Mission
Mode 3
Mode 1
Shift out
Shift in
ShiftDR
ClockDR
UpdateDR
C
U
BIDI Data Cell AC_8
Output Data
Pad
Mode 1
Shift out
Shift in
ShiftDR
ClockDR
UpdateDR
AC Mode
AC Test Signal
Input Data

11.7 AC_9



11.8 AC_10



12. BSCAN指令

12.1 SAMPLE

只sample采样 capture pin input & output值，而不能影响其input pin到内部逻辑值和output pin到PAD的状态。

12.2 PRELOAD

主要用来更新update DR的值，这个值在后面的测试指令作用下，将会直接被驱动到output PAD脚；如果值没有初始化，将不确定输出的是什么值。

一般后面会再跟一个EXTEST指令，将PRELOAD初始化的值驱动到output PAD上。